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INSTRUCTION MANUAL

EMR MODEL 515-03
PAM/PDM SYNCHRONIZER
(REVISION D)

EMR

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INSTRUCTION MANUAL

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(REVISION D)

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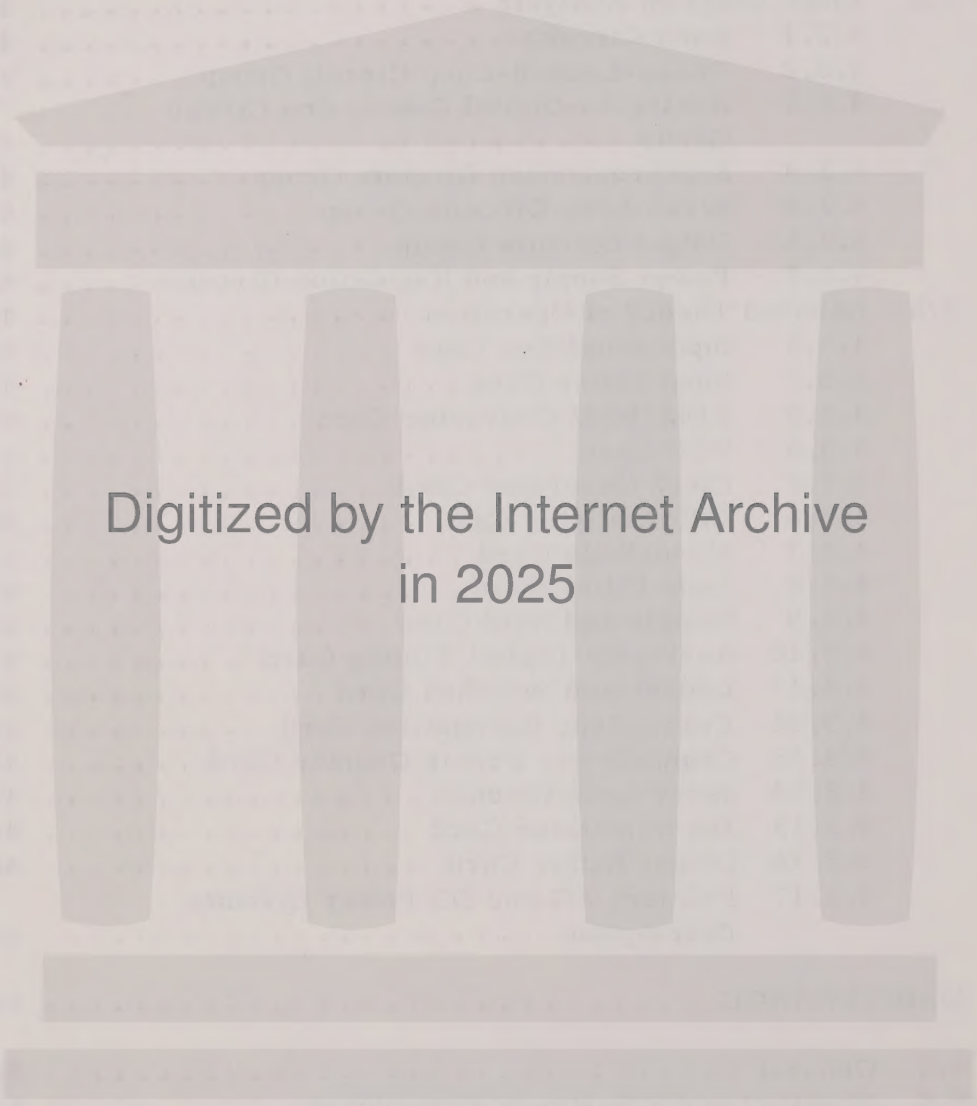
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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

This instruction manual provides information describing the operation and maintenance of the EMR Model 515 PAM/PDM Synchronizer. Included in this manual are functional and physical descriptions of the unit, specifications, installation and operating instructions, theory of operation, maintenance data, and parts lists.

The EMR Model 515 PAM/PDM Synchronizer is a complete unit which provides signal conditioning, synchronization, and data conversion capabilities for pulse-amplitude-modulated (PAM) input signals or pulse duration modulated (PDM) input signals. The Model 515 accepts either PAM-NRZ (non-return-to-zero) inputs at channel rates of from 10 channels per second to 100,000 channels per second, PAM-RZ (return-to-zero) inputs at channel rates from 10 channels per second to 50,000 channels per second, or PDM inputs at channel rates of 10 channels per second to 10,000 channels per second. The input data pulses are converted to digital form by means of a high-speed digital-to-analog converter. Full-scale and zero-scale servo loops are provided for automatic correction of offset and level variations in the incoming signal. A ten-bit, scaled digital output is provided at a rear-panel connector for subsequent routing to peripheral equipment such as an EMR Model 516 Demultiplexer or display devices. The Model 515 also contains facilities for decommutating a single, selectable channel from within a frame and providing an indication of the data value for the selected channel on a front panel meter as well as an analog output for the selected channel.

1.2 FUNCTIONAL DESCRIPTION (REF. FIGURE 1-1)

The function of the Model 515 PAM/PDM Synchronizer is to accept serial PAM or PDM input data from a receiver and to convert each data channel to an equivalent 10-bit, parallel output, binary data word. The Model 515 performs channel and frame synchronization and supplies this synchronization information with the output data. Also, any one channel of the input format may be selected for decommutation and provided as an analog output as well as being displayed on a front panel meter.

The serial input pulse train is conditioned in the input amplifier. When the input is initially applied to the Model 515, and before frame synchronization is acquired, the DC restorer provides an input to the amplifier which serves as a coarse offset adjustment. This maintains the zero data level at approximately the proper value. When frame synchronization is acquired, the DC restorer is inhibited and further adjustment of the offset is accomplished by the zero loop which is described later.

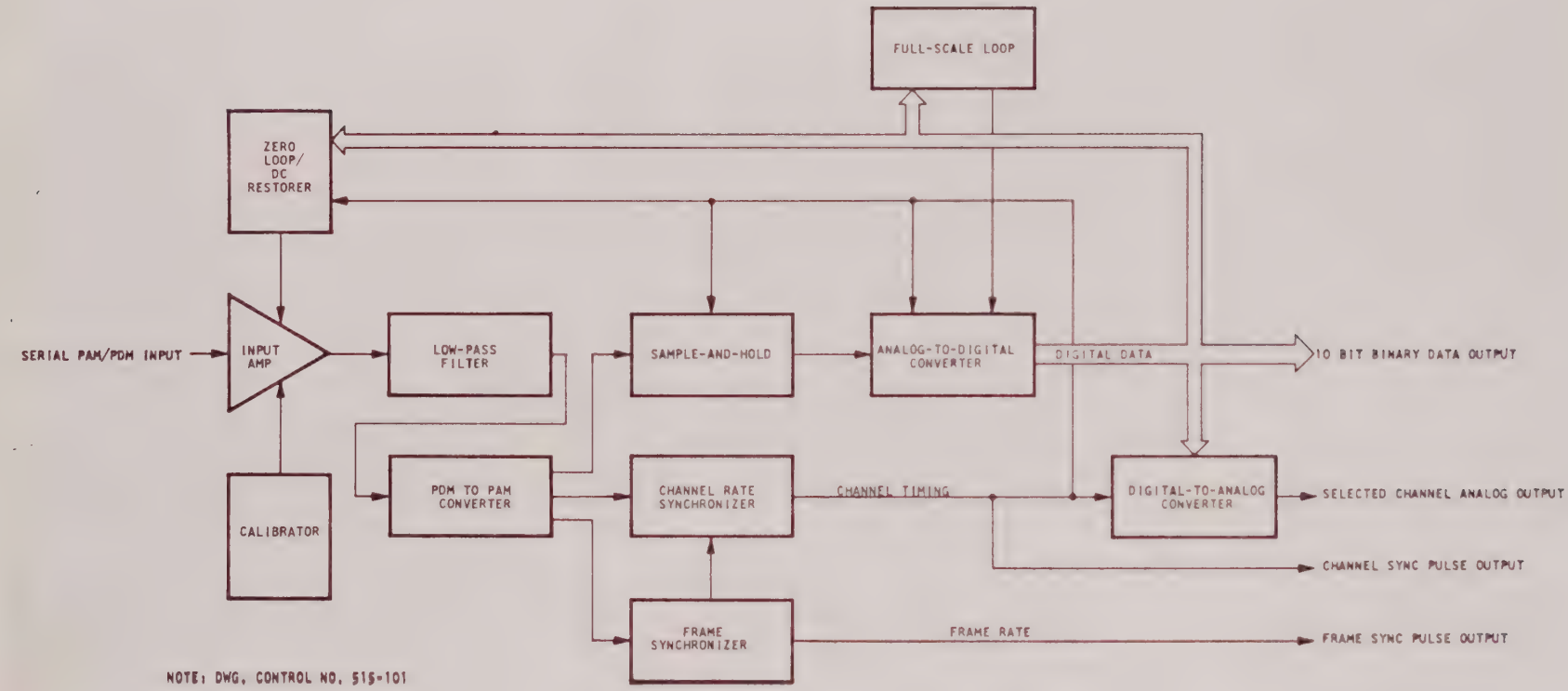


Figure 1-1. Model 515 Simplified Block Diagram

When receiving PAM-NRZ input signals with no pre-filtering, filtering is accomplished by means of a three-pole, Bessel type low-pass filter. The filter cutoff frequency is determined by front panel programming of the input channel rate. If pre-filtering is provided or when the input signal is in the form of either PAM-RZ code or PDM code, the low-pass filter is functionally bypassed by means of a front-panel toggle switch. The output from the low-pass filter is applied to a PDM-to-PAM converter. When the input signal is in PAM form the signal is gated directly through the converter and routed to the sample and hold, frame synchronization, and channel synchronization functions. If the input signal is received in a PDM format, the signal is converted to PAM form before distribution.

Channel synchronization is acquired and maintained by a phase-locked loop having two selectable loop widths, wide and narrow. The frame synchronizer recognizes the frame synchronization pattern programmed on the front panel switches and phases the internal counting and timing accordingly. The PAM data pulses are sampled and the analog data converted to digital form by means of the analog-to-digital converter. The 10-bit digital data output is applied to the rear panel output connector and to the zero and full scale servo loops. In the zero servo, the digital data for the zero scale reference channel (minimum data) is compared with a preset binary number representing the desired minimum data value. A signal proportional to the difference between the two digital values is applied to the input amplifier in such a manner as to offset the output level of the amplifier. In the full-scale servo loop the digital value of the full-scale reference channel (maximum data) is compared with a preset binary number representing the absolute maximum data level. The resulting difference signal output is used to vary the reference voltage of the analog-to-digital converter. By means of these two servo loops, the offset of the zero scale level into the A/D converter, as well as the gain of the converter, are varied in such a manner as to produce specific digital numbers at the output which represent zero and full scale data values. Intermediate data points are converted in proportion to the zero and full scale values.

The digital data output is also applied to a digital-to-analog converter. The function of this circuit is to convert to analog form any one channel within the input frame format. Selection of the channel to be decommutated is accomplished by means of front panel thumbwheel switches. The analog value of the selected channel is displayed on a front panel meter and also is made available for distribution at a rear panel connector. Since the holding circuitry for the digital-to-analog circuitry is digital, the holding time is essentially infinite.

A built-in calibrator circuit provides precision full-scale, half-scale, and zero-scale input levels. These levels may be used to check the operational status of the input amplifier, low-pass filter, sample and hold, analog-to-digital converter, zero and full scale servo loops and the digital-to-analog converter. The only functions not afforded a check by the calibrator circuit are the channel and frame synchronizers. The calibrator also provides convenient and accurate output levels which may be used for calibration of strip chart recorders.

1.3 PHYSICAL DESCRIPTION

The Model 515 is a precision built, solid-state instrument designed for mounting in a standard 19-inch EIA-type equipment rack. The overall dimensions of the unit including rear panel connectors but excluding front panel handles and components are 3-1/2-inches high, 19-inches wide, and 13-inches deep. The Model 515 weighs approximately 35 pounds excluding the slides.

The complete assembly diagram for the Model 515 is shown in Figure 5-1. For convenience in the presentation of wiring information, arbitrary reference designations have been assigned to the main chassis (A1), the front panel (A2), and the rear panel (A3). The main chassis contains the 19 plug-in printed-wiring board assemblies and an interconnection board. The main chassis is also the location of the self-contained power supply which provides all DC voltages required by the printed-wiring boards. The printed-wiring board connector locations are identified in Figure 1-2 and the card provided for each location is identified in Table 1-1. The front panel assembly, A2, contains all controls required to establish the operating parameters for the Model 515 and test points and indicators for monitoring the operational status. The front panel controls, indicators, and test points are identified and described in Section 3 of this manual. All input and output signal and power distribution connections for the Model 515 are made through connectors on the rear panel assembly, A3. These connectors are also identified in Section 3.

The 515 has a removable bottom cover for ease of access to chassis wiring for test and/or repair purposes.

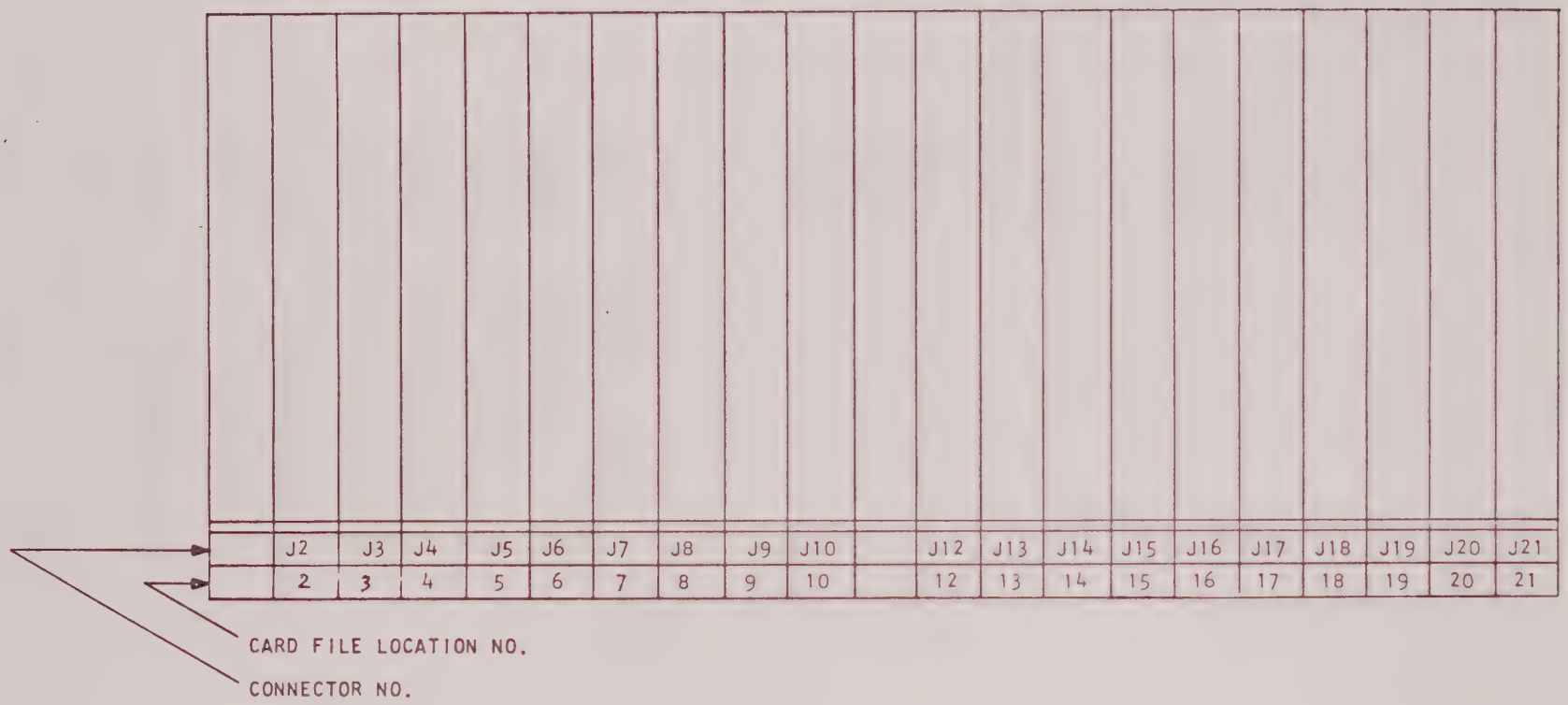


Figure 1-2. Printed-Wiring-Board Locations
(See Table 1-1)

Table 1-1. Model 515 Printed-Wiring Boards

CARD NO.	ASSY. NO.	PRINTED-WIRING BOARD NAME
1	---	Not used
2	18872	Output Buffer
3	18869	Decommutator
4	28090	Servo DAC
5	18889	Servo Adder
6	18886	Servo Control
7	18839	A/D Timing
8	18842	Ladder and Switches
9	18845	Sample and Hold
10	22852	Frame Sync Recognition
11	---	Not used
12	22066	Channel/Frame Counter
13	22063	Clock Generator
14	18854	VCO
15	18875	Loop Filter
16	18866	Monostable
17	18857	Differentiator
18	21808	PDM/PAM Converter
19	18863	Input Filter
20	18883	Input Amplifier
21	1373	Regulator

SECTION 2

SPECIFICATIONS

2.1 GENERAL

This section outlines the electrical and mechanical specifications for the EMR Model 515 PAM/PDM Synchronizer.

2.2 ELECTRICAL SPECIFICATIONS

2.2.1 Input Requirements

a. Signal Types (Figure 2-2):

1. 50% PAM RZ

2. 100% PAM NRZ

3. PDM

NOTE

For PDM inputs, the zero-scale reference channel may be represented by a pulse width of 5% to 15% of the channel period and the full-scale reference channel may be represented by a pulse duration of 45% to 70% of the channel period. The Model 515 may be adjusted to identify specific pulse durations within these ranges.

b. Level: 1.0 to 30 volts peak-to-peak. Manually adjustable.

c. DC Offset: Up to ± 50% of the peak-to-peak input level.

d. Input Impedance: At least 10k ohms shunted by no more than 150 pF.

e. Input Configuration: Single ended.

f. Polarity: Normal or inverted.

2.2.2 Channel Synchronization

a. Channel Rates (Front panel selectable to within 1% of the incoming channel rate):

1. PAM-NRZ: 10 to 100,000 channels per second.

2. PAM-RZ: 10 to 50,000 channels per second.

3. PDM: 10 to 10,000 channels per second.

b. Tracking: Two tracking positions are provided; wide (± 10% range and 3% loop width) and narrow (± 1% range and 3% loop width).

c. Acquisition Time: The time required to achieve synchronization with the incoming signal is less than 100 channel periods in the wide tracking position.

d. Transition Density: Synchronization will be maintained for frames with a length of up to 64 channels containing a standard IRIG frame sync pattern and no data transitions in the narrow tracking position.

e. Detectable Transition: Transitions of less than ± 20% of full scale will not be recognized when filter is on.

2.2.3 Frame Synchronization

a. PAM Frame Sync Formats: The frame synchronizer will recognize either of the following PAM formats:

1. PAM-RZ, 50 Percent Duty Cycle -- The synchronization interval shall be 1.5 channel periods in duration and of full-scale amplitude.

2. PAM-NRZ, 100 Percent Duty Cycle -- The synchronization interval shall be five channel periods in duration and shall consist of a zero amplitude level for one channel period followed by a full amplitude level for three channel periods followed by a 1/2, or less, amplitude level for the last channel period.

b. PDM Frame Sync Format: The frame synchronizer will recognize either of the following PDM formats:

1. A full amplitude pulse for a duration of 1.5 channels in a 2-channel time period.

2. The absense of a pulse for two channel periods.

c. Non-Standard: Combinations of 0, 1/2, or full-scale amplitude channels with durations up to 5 channels in PAM-NRZ, 3 channels in PAM-RZ, and 2 channels in PDM.

d. Frame Length: From 10 to 199 channels per frame.

e. Acquisition Time: On first frame sync pattern after channel synchronization is acquired.

f. Synchronization Modes: Search and lock modes are provided.

1. Search -- Searches for first frame sync pattern after channel sync is obtained.

2. Lock -- Maintains sync for two consecutive missing patterns, reverts to Search on third consecutive missing sync pattern.

2.2.4 Jitter

Synchronization is maintained with ±10% channel edge jitter.

2.2.5 Signal-to-Noise

a. PAM-NRZ: Synchronization is indicated not less than 50% of the time with a signal-to-noise ratio of 10 dB when signal and noise are band-limited at five times the channel rate. Signal is defined as the peak-to-peak voltage of the PAM input; noise is the rms voltage at the 515-03 input.

b. PDM: Synchronization is acquired and maintained with peak-to-peak noise equal to 98% of the peak-to-peak signal.

2.2.6 Data Accuracy

a. Linearity: ±0.15% of full-scale best straight line in PAM and in PDM up to 5 kch/s.

b. Crosstalk:

1. PAM, Filter Out -- ±0.1% of full scale.

2. PAM, Filter In -- ±0.3% of full scale.

3. PDM -- ±0.1% of full scale.

2.2.7 Digital Output

a. Signal Characteristics:

1. Logic Levels -- ZERO, 0V to +0.45V DC; ONE, +3V to +5V DC.

2. Output Current -- Each output can sink 20 mA maximum (V_{out} = 0 volt). Each output can supply 1.2 mA maximum (V_{out} = +3 volts).

3. Rise and Fall Times -- 12 nanoseconds maximum with maximum load at the output connector. (Measured between the 1- and 2-volt levels.)

b. Data Output: Ten parallel binary bits.

c. Channel Rate Pulse: A positive-going pulse with a minimum pulse width of 500 nanoseconds. Generated once per channel while the data is stable.

d. Frame Rate Pulse: A logic ONE pulse with a minimum pulse width of 500 nanoseconds. Generated once per frame and is terminated at least 100 nanoseconds before the Channel Rate Pulse for channel 1.

2.2.8 Analog Output

a. Quantity: One analog output is provided with front-panel channel selection. This analog value is also displayed on a front-panel meter.

b. Resolution: Ten bits.

c. Amplitude: ±5V (see Figure 2-3 for full scale, zero scale definition).

d. Output Current: ±10 mA maximum.

e. Output Impedance: 0.5 ohm maximum.

f. Linearity: ±0.05% of full scale.

g. Offset: ±0.05% of full scale.

h. Gain Accuracy: ±0.05% of full scale.

i. Stability:

1. Offset -- ±20 ppm/°C.

2. Gain -- ±20 ppm/°C.

j. Settling Time: Output settles to within ±0.1% of full scale of final value within 60 μsec.

2.2.9 Auto Correction

a. Accuracy: Zero and full-scale reference servos provide automatic scaling within ±LSB over the temperature range.

b. Correction Range: Zero and full-scale reference variations may be corrected up to ±20% of full scale.

c. Correction Rate: 40%, 70%, or 100% of the zero and full-scale errors are corrected per frame. An OFF position is also provided.

2.2.10 Filtering

A three-pole, constant time delay, input filter is provided for use with PAM-NRZ input signals. The filter cutoff frequency is equal to the programmed channel rate.

2.2.11 Calibration

An internal calibrator is provided for the selection of three-point DAC calibration (0%, 50%, and 100% of full scale).

2.2.12 Data Inhibit

Both digital and analog outputs are inhibited from updating before frame synchronization is acquired or after synchronization is lost.

2.3 POWER REQUIREMENTS

2.3.1 Input Voltage

a. Model 515-03-0: 105V to 130V rms at 47 to 65 Hz.

b. Model 515-03-8: 210V to 260V rms at 47 to 65 Hz.

2.3.2 Input Power

Not more than 100 watts.

2.4 MECHANICAL SPECIFICATIONS

a. Height: 3-1/2 inches.

b. Width: 19 inches.

c. Depth: 15 inches.

d. Weight: Approximately 35 pounds (excluding slides).

e. Mounting: See Figure 2-1.

f. Paint Finish: See Figure 2-1.

2.5 ENVIRONMENTAL SPECIFICATIONS

a. Operating Temperature: 0°C to +50°C.

b. Storage Temperature: -40°C to +80°C.

c. Relative Humidity: Up to 95%.

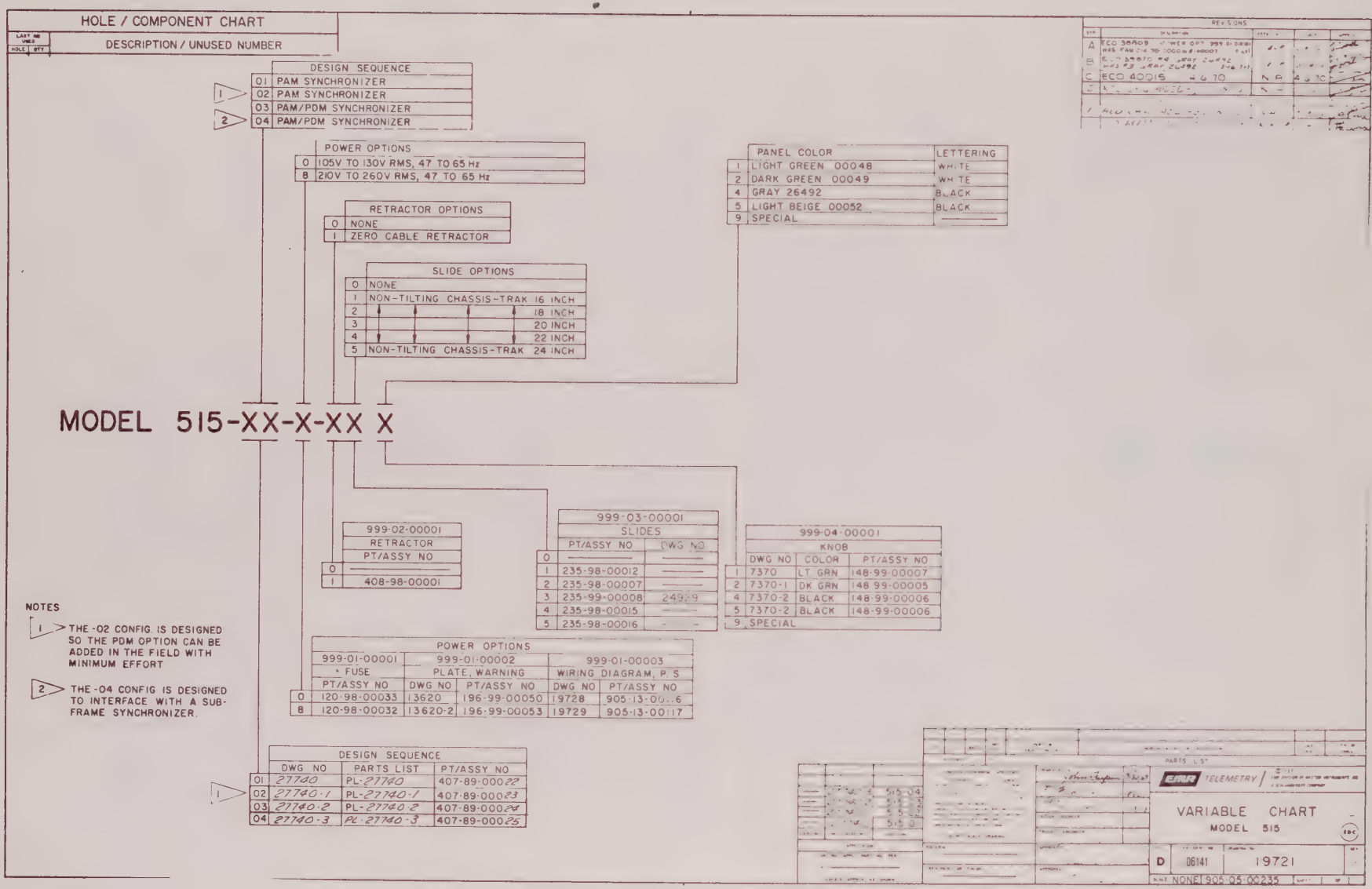


Figure 2-1. Model 515 PAM/PDM Synchronizer Variable Chart

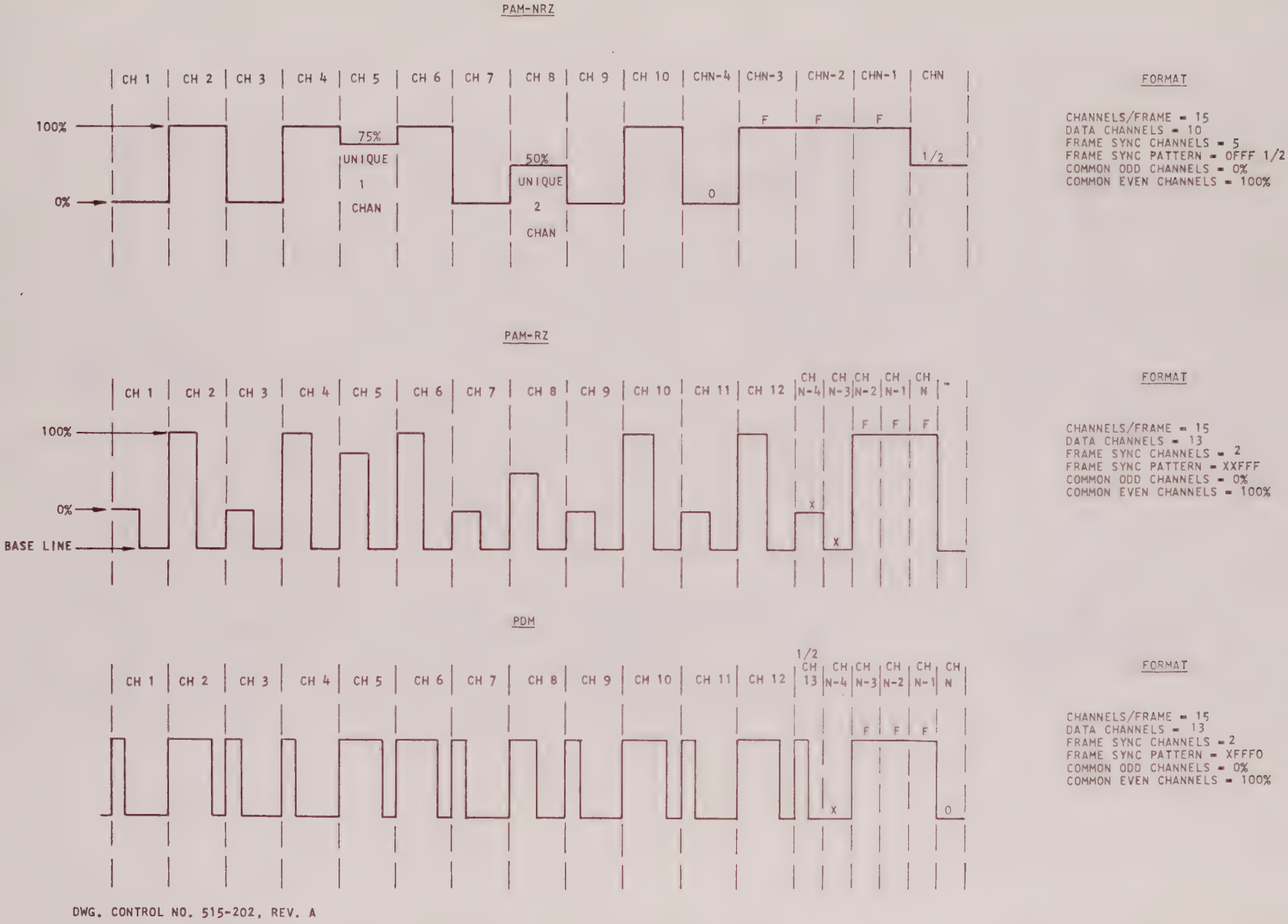


Figure 2-2. Typical Input Formats for PAM-NRZ, PAM-RZ, and PDM

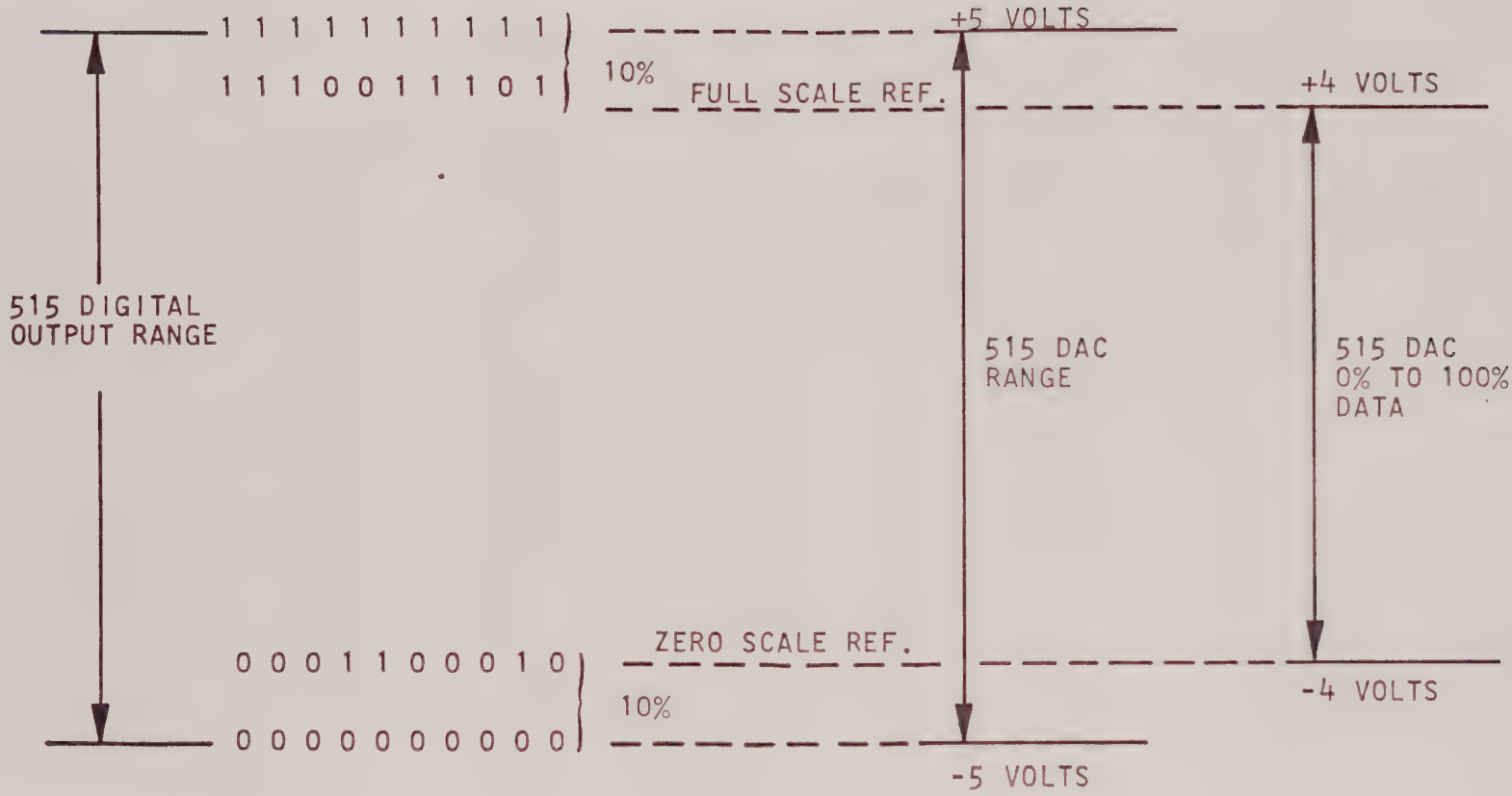


Figure 2-3. Model 515 Digital Output/Analog Output Relationship

SECTION 3

INSTALLATION AND OPERATION

3.1 INSTALLATION

The EMR Model 515 PAM/PDM Synchronizer is shipped completely assembled and ready for installation. The unit is calibrated and adjusted prior to shipment and all plug-in printed-wiring cards inserted into the appropriate receptacles and all covers installed. The unit should be inspected immediately on its arrival and notice given to EMR-Telemetry of any claim that the product does not conform with the terms of the order.

The Model 515 may be ordered with or without mounting slides. Units ordered without slide mounts may be bolted directly to a standard 19-inch, EIA-type equipment rack with the hardware provided for that purpose. For installation of a Model 515 with slide mounts, remove the slides from the synchronizer after unpacking the unit and mount the slides to the internal frame of the equipment rack. Mounting hardware for this installation is supplied with the synchronizer. Insert the synchronizer into the slides until the unit is firmly seated. Turn-to-lock fasteners located on either side of the front panel secure the unit in the rack.

The Model 515 may be extended from the equipment rack for servicing by loosening the front-panel turn-to-lock fasteners and pulling the unit straight out. Push-button stop latches, located on the outside surfaces of both slides, hold the unit at the maximum extension. At this point, the Model 515 may be removed from the rack by depressing the pushbutton stop latches and pulling the unit straight out.

The external electrical connections to the Model 515 are terminated at connectors on the rear panel. These connectors and other rear-panel components are illustrated in Figure 5-1 and described in Table 3-1.

3.2 OPERATION

3.2.1 Front Panel Operating Controls and Indicators

All operating parameters for the Model 515 are manually programmed using the front-panel control switches. Figure 3-1 identifies all front-panel controls, indicators, and test jacks and Table 3-2 defines the function of each control, indicator, or test jack. Detailed descriptions of channels/frame selection and frame sync selection are furnished in paragraphs 3.2.2. and 3.2.3.

3.2.2 Channels/Frame Selection

The number of channels to occur in each frame is selected by the front-panel CHANNELS/FRAME thumbwheel select switches. When selecting the channels/frame, the required number of data channels is added to the number of frame-sync

channels. The number of frame-sync channels in each frame is dependent on the operating mode of the 515-03 as follows:

a. Up to five channels are available in the PAM-NRZ mode.

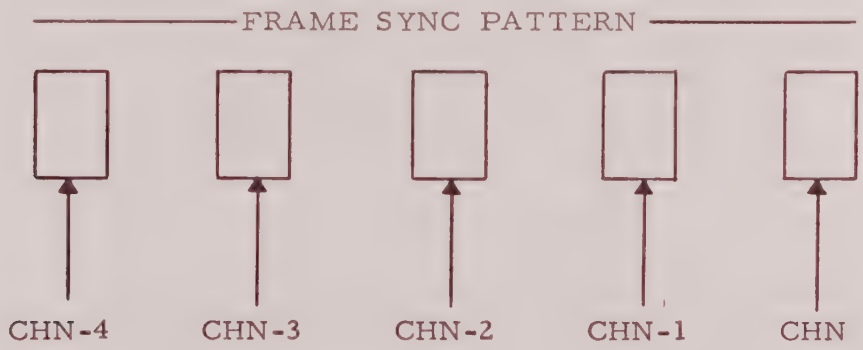
b. Up to 2-1/2 channels are available in the PAM-RZ mode.

c. Up to two channels are available in the PDM mode.

If less frame-sync channels are required by the format, the appropriate FRAME SYNC PATTERN switches can be set to X which is a "don't care" position. These channels then become data channels in the format.

3.2.3 Frame-Sync Pattern Selection

The frame-sync channels and the channel patterns are selected by the front-panel FRAME SYNC PATTERN switches. In the PAM-NRZ mode, five switches select the patterns in five frame-sync channels. In the PAM-RZ and PDM modes, these five switches set the patterns in three frame-sync channels. Each switch is assigned a unique identifier as follows:



3.2.3.1 PAM-NRZ Mode

In this mode, up to five sync patterns for the last five channels in a frame are selected by the pattern switches. Each switch sets the pattern for a full channel period. The channel period is the same as the data channel period. A typical pattern is shown in Figure 2-2 which also illustrates the data channel selections. If less than five sync channels are required, the switches (starting from the left at CHN-4) are set to position X which is a "don't care" position. In this position, the sync channels become data channels.

3.2.3.2 PAM-RZ Mode

In this mode, up to five sync patterns for the last three channels in a frame are selected by the pattern switches. Each switch sets the pattern for one-half of a channel period. The last half of the last channel (CHN) is not selectable and always returns to baseline.

If only two channels are required in the frame-sync pattern, pattern switches N-4 and N-3 are set to position X which is a "don't care" position. In this position, the sync channel becomes a data channel.

3.2.3.3 PDM Mode

In this mode, up to two sync patterns are selected by the pattern switches. A typical frame-sync pattern (a full-amplitude pulse for a duration of 1.5 channels in a 2-channel period) is illustrated in Figure 2-2.

3.2.4 Operating Procedures

Operation of the Model 515 PAM/PDM Synchronizer is fully automatic once the front-panel switches are programmed in accordance to the parameters of the input format and power is applied to the unit. The following procedures may be used as a guide for the operational setup of the Model 515:

a. Operation With PAM Inputs:

1. Verify that all rear panel input and output connectors are secure and mated to appropriate peripheral equipment. (See Figure 3-1 and Table 3-1.)

NOTE

The controls and indicators referenced in the following steps are all located on the front panel of the Model 515 (see Figure 3-2 and Table 3-2).

2. Set the MODE switch (17) to PAM.

3. Set the CHANNELS/FRAME thumbwheel switches (2) for the number of channels per frame of the input format.

4. Set the ZERO REF CHAN thumbwheel switches (3) for the channel number of the input format containing the zero reference data.

5. Set the FS REF CHANNEL thumbwheel switches (4) for the channel number of the input format containing the full scale reference data.

6. Set the CODE switch (16) to RZ or NRZ as applicable for the code type of the input signal.

7. Set the FILTER switch (15) to OUT if the input signal code is RZ or if pre-filtering is employed. Set the FILTER switch to IN if the input data is in PAM-NRZ code with no pre-filtering.

8. Set the TRACK switch (14) to NAR.

9. Set the POL switch (13) to NORM or INV as applicable to agree with the polarity of the input data.

10. Set the CHANNEL RATE thumbwheel switches (18) for the frequency of the input data pulses.

11. Set the FRAME SYNC PATTERN thumbwheel switches (19) in accordance to the synchronization pattern of the input format. For the conventional five-channel PAM-NRZ sync pattern, set the pattern switches as follows:

O F F F 1/2

NOTE

The RZ synchronization code employs split channel coding with two code values programmed for each channel. The last half of the last channel is not part of the sync pattern.

For the two-channel PAM-RZ sync pattern, set the switches as follows:

X X F F F

For the three-channel PAM-RZ sync pattern, set the switches as follows:

F F F F F

12. Set the CALIBRATOR switch (10) to OFF.

SERVO - OFF/40/70

13. Depress the POWER switch (11) to apply power to the Model 515.

14. Adjust the INPUT potentiometer (9) to the point at which the INPUT meter (8) provides a mid-scale (green band) indication. The ZERO (21) and FS (20) indicators should be extinguished.

ZERO - HIGH/LOW
FS

NOTE

If the quality of the input signal is poor (low signal-to-noise ratio), use the FRAME SYNC indicator (1) as the guide for setting the INPUT potentiometer. Adjust the potentiometer to the point at which the indicator will extinguish. This will provide an indication on the INPUT meter above the green band region.

15. Set the SERVO switch (12) in accordance to the quality of the input signal. With a high signal-to-noise ratio input, the SERVO switch may be set to 100%. With a low signal-to-noise ratio, the switch should be set to a lower correction rate.

b. Operation With PDM Inputs:

1. Verify that all rear panel input and output connectors are secure and mated to appropriate peripheral equipment. (See Figure 3-1 and Table 3-1.)

NOTE

The controls and indicators referenced in the following steps are all located on the front panel of the Model 515 (see Figure 3-2 and Table 3-2).

2. Set the MODE switch (17) to PDM.

3. Set the CHANNELS/FRAME thumbwheel switches (2) for the number of channels per frame of the input format.

4. Set the ZERO REF CHAN thumbwheel switches (3) for the channel number of the input format containing the zero reference data.

5. Set the FS REF CHANNEL thumbwheel switches (4) for the channel number of the input format containing the full scale reference data.

6. Set the CODE switch (16) to NRZ.

7. Set the FILTER switch (15) to OUT.

8. Set the TRACK switch (14) to WIDE or NAR as desired.

9. Set the POL switch (13) to NORM or INV as applicable to agree with the polarity of the input data.

10. Set the CHANNEL RATE thumbwheel switches (18) for the frequency of the input data pulses.

11. Set the FRAME SYNC PATTERN thumbwheel switches (19) in accordance with the synchronization pattern of the input format as follows:

    (a) IRIG two-channel, 1.5-channel duration --

        X F F F O

    (b) IRIG two-channel missing pulse, 2-channel duration --

        X O O O O

12. Set the CALIBRATOR switch (10) to OFF.

13. Depress the POWER switch (11) to apply power to the Model 515.

14. Adjust the INPUT potentiometer (9) to the point at which the INPUT meter (8) provides a mid-scale (green band) indication.

15. Set the SERVO switch (12) to the 40% correction rate. The FRAME/CHAN SYNC indicators (1), FS indicators (20), and ZERO indicators (21) should be extinguished.

Table 3-1. Function of Rear Panel Connectors
(See Figure 5-1)

REF. NO.	NAME	TYPE	FUNCTION
P1		Hubbell Twist-lock	Primary input power connection point
J1		32-Pin	Output connector for distribution of 10-bit binary data output, channel rate pulse, and frame rate pulse to external equipment
J2		Binding Post	Chassis ground connection
J3		Binding Post	Signal ground connection
J4		BNC	Serial input jack
J5		BNC	Decommutated channel output

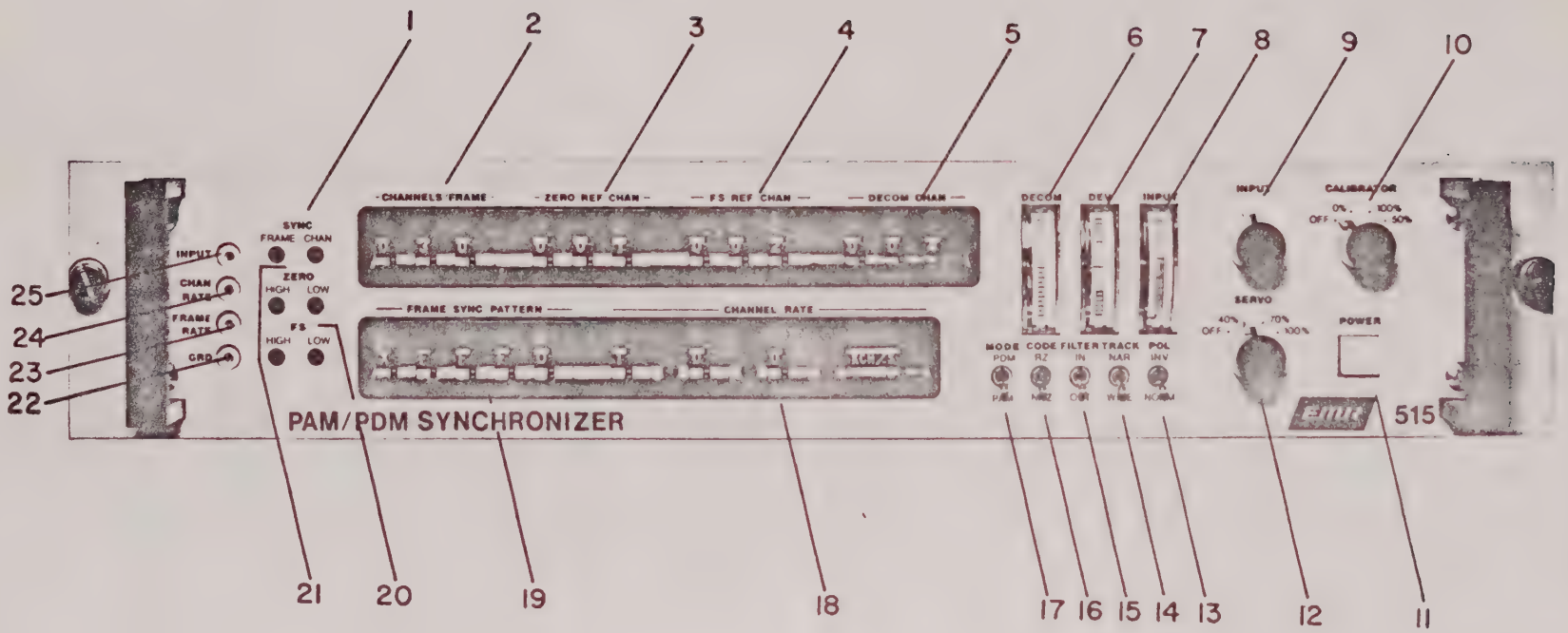


Figure 3-1. Model 515-03 Front Panel Operating Controls and Indicators

Table 3-2. Function of Front Panel Controls and Indicators
(Ref. Figure 3-1)

REF. NO.	NAME	DESIG-NATION	FUNCTION
1	SYNC/FRAME Indicator	DS4	When extinguished indicates frame synchronization has been achieved.
	CHAN Indicator	DS1	When extinguished indicates channel synchronization has been achieved.
2	CHANNELS/ FRAME Thumb-wheel Switches	S17 thru S19	Provide for selection of frame length (10 to 199 channels per frame), including frame-sync pattern.
3	ZERO REF CHAN Thumbwheel Switches	S14 thru S16	Provide means of identifying the zero scale reference channel of the input format. Adjustable from 1 to 199.
4	FS REF CHAN Thumbwheel Switches	S11 thru S13	Provide means of identifying the channel containing the full scale reference input. Adjustable from 1 to 199.
5	DECOM CHAN	S8 thru S10	Provides means of selecting any channel of the input frame format for display on the front panel and output at rear-panel connector J5.
6	DECOM Meter	M3	Provides indication of analog value of channel selected for decommutation.
7	DEV Meter	M2	Indicates difference in frequency between internal clock and the front panel selected channel rate. White area indicates ± 10% deviation limits when TRACK switch A2S5 is in the WIDE position and ± 1% limits with A2S5 in the NAR position.
8	INPUT Meter	M1	Indicates peak-to-peak magnitude of input signal.
9	INPUT Potenti-ometer	R1	Used to attenuate input signal. When properly adjusted, INPUT meter reads center scale.

Table 3-2 (Cont'd.). Function of Front Panel Controls and Indicators (Ref. Figure 3-1)

<table>
<tr><th>REF. NO.</th><th>NAME</th><th>DESIG-NATION</th><th>FUNCTION</th></tr>
<tr><td>10</td><td>CALIBRATOR Switch</td><td>S1</td><td>In 0%, 100%, and 50% positions, all data channels are strobed to the calibration voltage levels listed below (SERVO switch must be in a position other than OFF). When the CALIBRATOR switch is in the OFF position, the input signal is applied to the 515 for normal operation.

Pos. — Calibrator Voltage
OFF — Bypassed
0% — −0.4V (Zero Scale)
100% — +0.4V (Full Scale)
50% — Grd (Mid-Scale)</td></tr>
<tr><td>11</td><td>POWER Push-button Indicator/ Switch</td><td>S2/DS10</td><td>When lit, indicates primary AC power is applied to unit. Depress to actuate.</td></tr>
<tr><td>12</td><td>SERVO Switch</td><td>S3</td><td>Selects the percentage of zero-scale and full-scale servo correction to be made during each frame. In the OFF position, the servos are not operative.</td></tr>
<tr><td>13</td><td>POL Toggle Switch</td><td>S4</td><td>Normal polarity is defined as meaning that increasing data value produces an increasing voltage at the input of the Model 515. The INV position of switch A2S4 is used for input signals of the opposite sense.</td></tr>
<tr><td>14</td><td>TRACK Toggle Switch</td><td>S5</td><td>Selects allowable percentage of frequency change with respect to programmed input channel rate and the maximum rate of tracking as follows:

Pos. — Max. Change — Max. Rate of Tracking
NAR — 1% — 0.3%
WIDE — 10% — 3.0%</td></tr>
</table>

Table 3-2 (Cont'd.). Function of Front Panel Controls and Indicators (Ref. Figure 3-1)

REF. NO.	NAME	DESIG-NATION	FUNCTION
15	FILTER Toggle Switch	S6	In the IN position, a 3-pole, constant-delay filter is placed in the signal path. Filter cutoff is set to channel rate. This filter is used only in PAM/NRZ when no pre-filtering is provided. When in PAM/RZ or PDM format, the filter must be placed in the OUT position which removes it from the signal path.
16	CODE Toggle Switch	S7	Set to identify type of code (RZ or NRZ) in which the input data signal is received. NOTE Switch S7 must be in the NRZ position for PDM mode of operation.
17	MODE Toggle Switch	S29	Set to identify the type of input signal, PAM or PDM.
18	CHANNEL RATE Thumbwheel Switches	S20 thru S23	Select the 515 channel rate (10 ch/sec to 100 kch/sec). A number other than zero must be set into the most significant digit position.
19	FRAME SYNC PATTERN Thumbwheel Switches	S24 thru S28	Select the expected level of each channel in the frame-sync pattern. An X selected is a "don't care" level, a 0 selected is a 0% level, a 1/2 selected is a 50% level, and an F selected is a 100% level.
20	FS/HIGH	DS6	When lit, indicates full scale reference channel level is too high.
	FS/LOW Indicator	DS3	When lit, indicates full scale reference channel level is too low.

Table 3-2 (Cont'd.). Function of Front Panel Controls and Indicators (Ref. Figure 3-1)

REF. NO.	NAME	DESIG-NATION	FUNCTION
21	ZERO/HIGH Indicator	DS5	When lit, indicates zero scale reference channel level is too high.
	ZERO/LOW Indicator	DS2	When lit, indicates zero scale reference channel level is too low.
22	GRD Test Jack	TP1	Ground test point.
23	FRAME RATE Test Jack	TP2	A positive pulse with a minimum width of 500 nsec (TTL levels) that occurs once per frame. This pulse terminates a minimum of 100 nsec preceding the channel rate pulse for channel 1. This output is short-circuit proof.
24	CHAN RATE Test Jack	TP3	A positive pulse with a minimum width of 500 nsec (TTL levels) that occurs once per channel while output data is stable. This output is short-circuit proof.
25	INPUT Test Jack	TP4	The input signal after passing through the input amplifier. Nominal signal levels at this point are +3 to +7 volts. This test point is short-circuit proof.

SECTION 4

THEORY OF OPERATION

4.1 GENERAL

This section contains the functional theory of operation for the Model 515 PAM/PDM Synchronizer. Theory discussions are provided at two levels; an overall block diagram description based on the system block diagram, Figure 4-1, is provided in paragraph 4.2 and individual descriptions for each of the printed-wiring boards contained in the Model 515, referenced to appropriate functional block diagrams, are provided in paragraph 4.3. Timing diagrams are provided where deemed necessary for understanding of complex circuits. Assembly and schematic diagrams and interconnection wiring lists for the Model 515 are located in Section 5 of this manual.

4.2 BLOCK DIAGRAM ANALYSIS

The Model 515 PAM/PDM Synchronizer conditions, synchronizes and converts each channel of a serial PAM-NRZ, PAM-RZ, or PDM input signal format to representative 10-bit binary words. The binary data words, plus channel and frame rate pulses and a synchronization status level, are provided as outputs for distribution to associated devices used in a PAM/PDM data processing system. The Model 515 also provides the capability of decommutating any one channel of the data format and converting the selected channel data to analog form for display on a front-panel meter. The analog value of the decommutated channel is also provided as an output of the Model 515.

The operational functions of the Model 515 PAM/PDM Synchronizer are performed by logic circuits contained on the printed-wiring cards. As shown in Figure 4-1, the 19 printed-wiring cards of the Model 515 are divided into six functional circuit groups with the operating parameters for the individual circuit groups being manually selected by front-panel controls. The general operation of each circuit group is discussed in the following paragraphs.

4.2.1 Input Circuits

The input circuits group is composed of input amplifier card 20, input filter card 19, PDM-to-PAM converter card 18, and the associated front-panel controls and indicators. The function of this circuit group is to condition the input data signal to provide signal characteristics compatible to operation of the other circuits groups of the Model 515. Input signal amplitudes of from 1 volt peak-to-peak to 30 volts peak-to-peak, representing minimum data to maximum data range, may be applied to the Model 515. The input signal is coupled through INPUT potentiometer A2R1 which is adjusted to attenuate the input to approximately 0.8 volts peak-to-peak (ideally, -0.4 volts to +0.4 volts). Proper adjustment of potentiometer A2R1 is indicated by a green-band reading on the

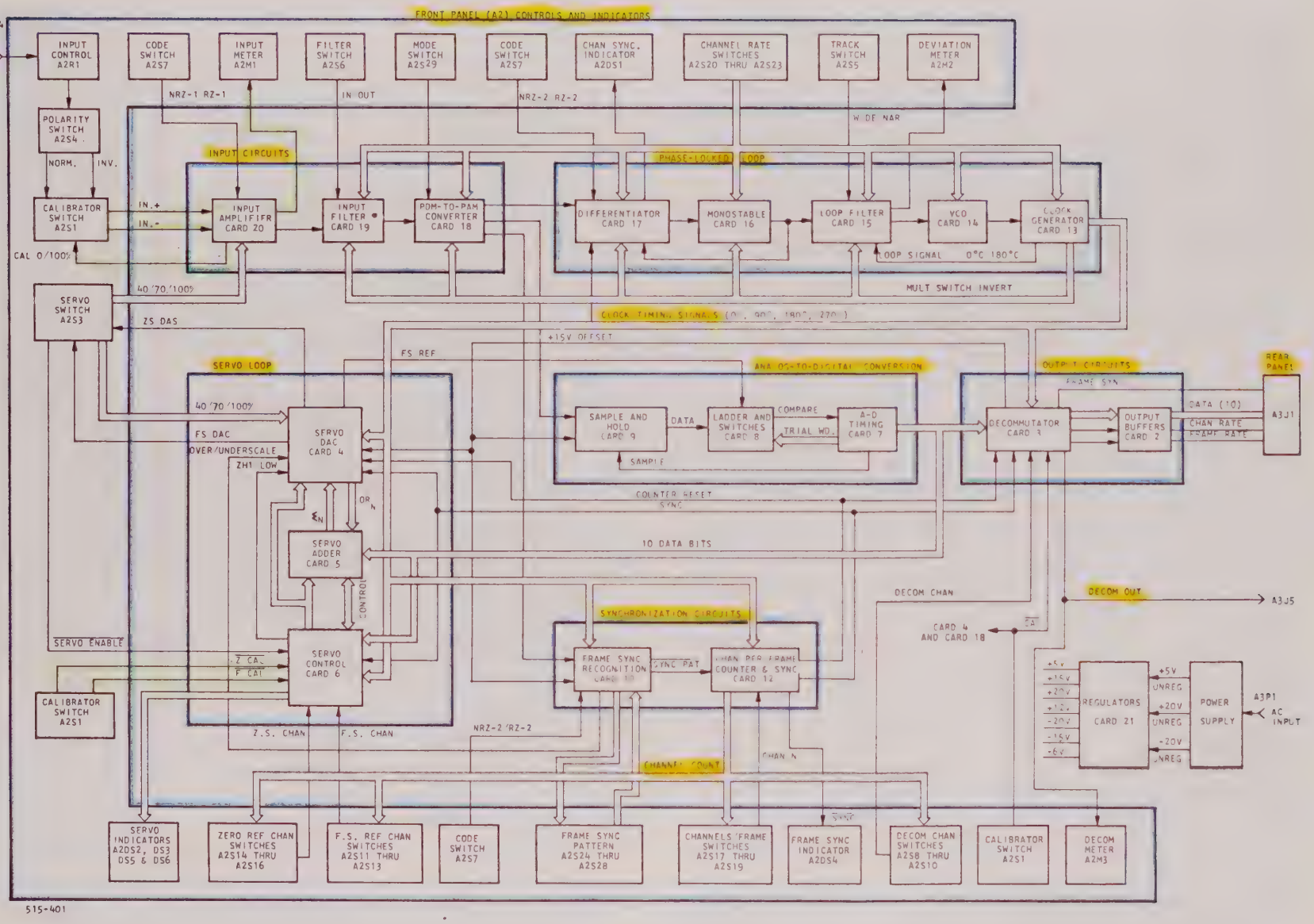


Figure 4-1. Model 515 Detailed Block Diagram

peak-detecting INPUT meter A2M1. The attenuated input signal is coupled through polarity (POL) switch A2S4 and CALIBRATOR switch A2S1 to the input amplifier card. Input conditioning is accomplished by a precision operational amplifier (gain of 5) which amplifies, level shifts, and inverts the input signal. The resultant output from card 20 provides a 4-volt peak-to-peak transition from the minimum data level (+7 volts) to the maximum data level (+3 volts). The conditioned data is applied to input filter card 19 which consists of a three-pole Bessel-type low-pass filter. The filter cutoff frequency is determined by the input channel rate programmed on the front-panel switch. If the input data is in either a PAM-RZ or PDM code format, the filter circuit is functionally bypassed by allowing all frequencies to pass. This is accomplished by setting the front-panel FILTER switch, A2S6, to the OUT position. The output from card 19 is applied to PDM/PAM converter card 18. The function of the PDM-to-PAM converter card is to condition PDM input signals in order to provide PAM-type signals to the phase-locked-loop circuit group, the analog-to-digital conversion circuit group and the frame synchronization circuit group. Card 18 couples an analog voltage level in the range of +3 volts to +7 volts to the analog-to-digital conversion function for each channel of the PDM input. A differentiated pulse is generated at the beginning of each PDM data channel and applied to the phase-locked-loop circuit group and a filtered PDM data signal is applied to the synchronization circuits. When operating a Model 515 PAM/PDM Synchronizer in the PAM mode, the input signal is switched directly through card 18 to the appropriate circuit groups.

The input data applied to the Model 515 may be either normal (signal level positive-going for increasing data) or inverted (signal level negative-going for increasing data). The polarity switch, A2S4, is positioned for the type of input data (NORM or INV) causing the input signal to be routed to the (–) or (+) input terminals, respectively on card 19. In the NORM position of switch A2S4, the input signal passes through three stages of inversion whereas in the INV position the input is inverted twice. Thus, the function of the polarity switching circuitry is to allow the same internal circuits to be used for processing both normal and inverted input data.

A calibrator circuit located on the input amplifier card produces three precision output levels (+0.4 volts, 0 volts, and –0.4 volts) which represent 100 percent, 50 percent, and 0 percent data levels, respectively. These precise voltages which are individually selectable by CALIBRATOR switch A2S1 are used to perform a three point calibration of the Model 515 data processing circuits and the external devices driven by the 515.

Compensation for DC offset of the input signal is also accomplished on the input amplifier card. The Model 515 has the capability of correcting for offsets of up to ±50 percent of the peak-to-peak input level. Offset correction is accomplished by applying an appropriate bias level to the input amplifier card from the servo loop circuit group. The operation of this function is discussed more fully in paragraph 4.2.5.

4.2.2 Phase-Locked-Loop Circuit Group

The phase-locked-loop circuit group is composed of differentiator card 17, monostable card 16, loop filter card 15, voltage-controlled oscillator card 14, and clock generator card 13. The function of this circuit group is to generate the internal channel rate timing signals used in sampling and conversion of the input data and to establish and maintain synchronization of the timing signals with the input data.

The internal clock timing signals are produced by the circuits on VCO card 14 and clock generator card 15. The VCO card contains an astable multivibrator with a self-starting circuit. The output frequency range of the VCO is variable within the range of 200 kHz to 2 MHz with the specific output frequency being a function of the channel rate digits programmed on the front panel CHANNEL RATE switches. The VCO output is applied to the clock generator card which, also under control of the CHANNEL RATE switches, divides the VCO frequency down to the programmed channel rate. The resultant channel rate signal is used to generate four square-wave timing signals; 0° clock, 90° clock, 180° clock and 270° clock. These four signals provide the primary internal timing for synchronization and conversion of the input data. The clock generator card also produces three strobe pulse outputs ($0^{\circ}S$, $\overline{180^{\circ}S}$, and $\overline{270^{\circ}S}$) which are derived from the corresponding square-wave signals. The loop signal routed from card 13 to the loop filter card is either the 0° clock (PDM or PAM-NRZ modes of operation) or the 180° clock (PAM-RZ mode of operation) as determined by the setting of CODE switch A2S7.

Synchronization of the internally-generated channel-rate timing signals to the signal input is acquired and maintained by the circuits located on differentiator card 17, monostable card 16, and loop filter card 15.

Before discussing the synchronization of the internal clock timing pulses with the input data, some of the timing relationships employed in the Model 515 must be understood. Under normal conditions, the ideal time to sample input data is at mid-data point. This allows equal time for allowing the input to stabilize before being sampled and for processing the data after sampling. For PAM-NRZ and PDM signals, the mid-data point is at 180° of the channel period whereas for PAM-RZ inputs the mid-data point is at 90° of the channel period. (Refer to Figure 4-2.) The timing pulses produced by the clock generator card are based on this relationship.

However, PAM-NRZ and PDM input data to the Model 515 is not stabilized until approximately the 270° point of the channel period due to the characteristics of the input filter. In order to maintain the conventional 180° sample time, the channel period for PAM-NRZ and PDM inputs is phase shifted 90° forward with respect to the 0° clock. Thus, the input data channel periods are coincident with the 270° internal clock and the 180° sample time occurs at a point (270° of the input channel period) at which the data is stable.

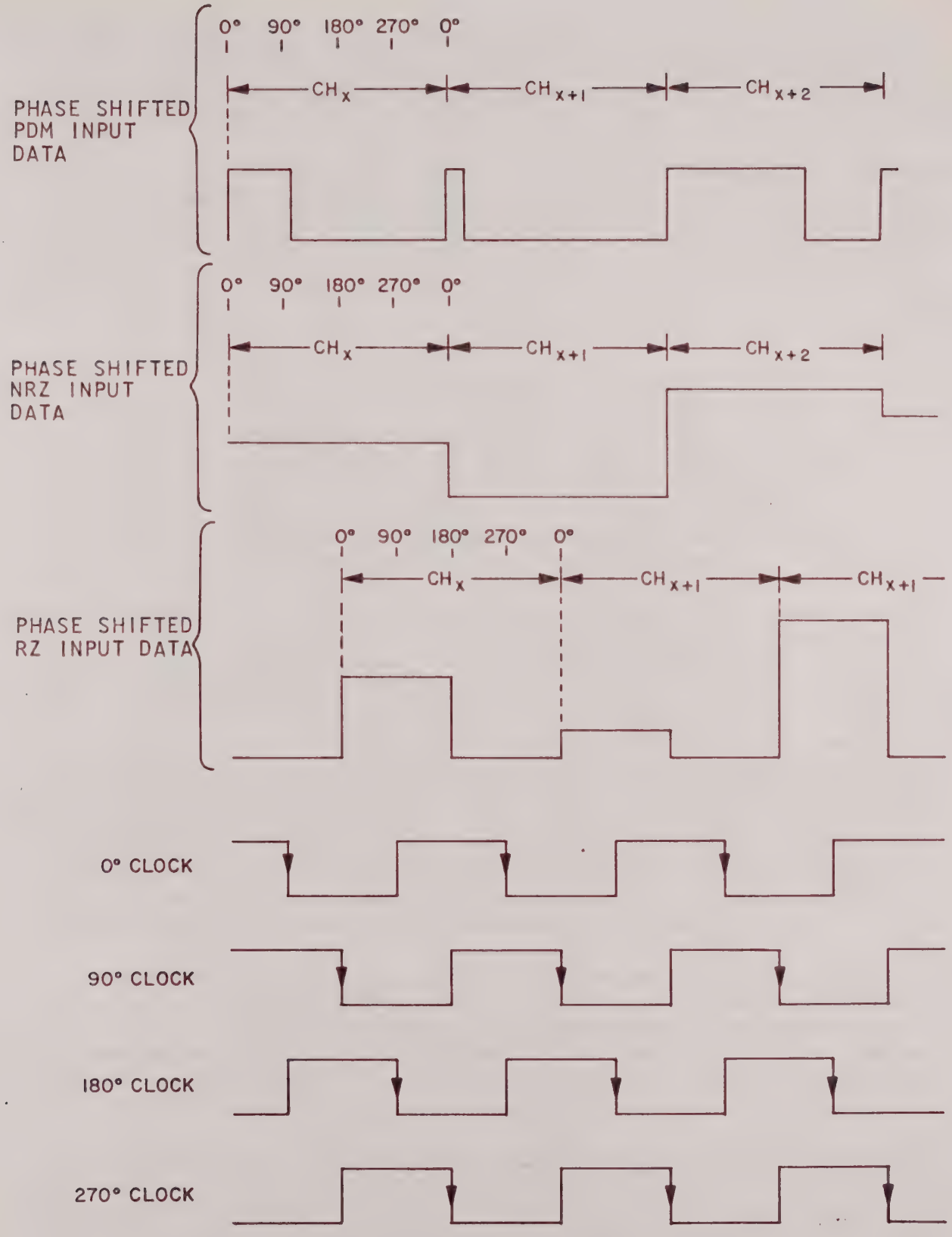


Figure 4-2. Input Signal vs Internal Clock Phase Relationships

In order to use the same timing for sampling and processing all input data formats, the phase of an PAM-RZ input signal is shifted to lag the 0° clock by 90 degrees. Thus, the data period for the 50 percent duty cycle PAM-RZ input extends from 90° to 270° and the mid-data point is coincident with the 180° clock.

When operating in the PAM mode, differentiator card 17 receives the conditioned PAM input from PDM/PAM converter card 18 and produces a positive-going pulse for each data level transition of ±20 percent or greater between adjacent channels of the input data. These pulses provide the input triggers for monostable card 16.

NOTE

Since the baseline reference for PAM-RZ data is approximately 20 percent below the minimum data level, two differentiated pulses may be generated for each channel of PAM-RZ coded inputs. Control inputs from CODE switch A2S7 inhibit the outputting of the pulses generated for the return-to-zero transition at mid-channel time when operating in the PAM-RZ mode.

When operating with PDM-coded input data, the PDM/PAM converter card furnishes a negative-going differentiated pulse to differentiator card 17 at the beginning of each channel period. Card 17 inverts the input pulse to provide a positive-going pulse trigger to the monostable card. Thus, each pulse applied to the monostable card represents the initiation of a new channel period although a pulse is not necessarily produced for each channel due to the ±20 percent data level transition requirement. The differentiator card also contains the channel synchronization detection circuitry. This circuit compares the phase relationship of the monostable output with the 270° clock timing signal in PAM-NRZ or PDM modes of operation and with the 90° clock signal in PAM-RZ mode of operation. (See Figure 4-2.) If the signals are not within the comparison limits, as averaged over several channels, a DC return is applied to CHAN SYNC indicator A2DS1 which causes the indicator to light.

The monostable card produces a negative-going output pulse for each input pulse trigger received from the differentiator card. The pulse duration is determined by switchable RC combinations which are controlled by the channel rate programmed on the front panel CHANNEL RATE switches. The RC combination selected for each channel rate is such as to provide a monostable output pulse width of approximately one-half of a channel period.

The monostable output is applied to the differentiator card for use in monitoring channel synchronization as described previously and is also coupled to loop filter card 15. The loop filter card provides the channel synchronization control for the Model 515 by providing frequency correction signals to the voltage-controlled oscillator. Card 15 is composed primarily of a phase detector and

an operational amplifier. During PAM-NRZ or PDM operation, the detector compares the monostable output with the 0° clock signal and during PAM-RZ operations, the monostable is compared with 180° clock signals. As shown in Figure 4-2, the compared signals in each mode of operation have a 90° phase relationship. If the phase relationship is correct, a 0-volt correction is applied to the VCO. If the frequency of the clock generator increases or decreases, the phase error is detected and a correction signal is routed to the VCO. This signal produces a VCO frequency change of equal magnitude but opposite polarity to the detected error.

Front panel DEV meter A2M2 provides a relative indication of deviation between the compared signals. Frequency variable components of the loop filter card are selected as a function of the front panel CHANNEL RATE switches. The front panel TRACK switch A2S5 controls the frequency deviation tracking capabilities.

4.2.3 Analog-to-Digital Conversion Circuit Group

The analog-to-digital conversion circuit group converts each channel of the analog input data into a parallel 10-bit binary-weighted data word. This function is accomplished by the circuits contained on sample and hold card 9, ladder and switches card 8, and analog-to-digital timing card 7.

The sample and hold card receives the analog data from PAM/PDM converter card 18 and amplifies, level-shifts, and stores the data value. The +3 to +7 volt maximum-to-minimum data range output from card 18 is doubled, +6 to +14 volts, and level shifted to -9 to -1 volts. The full range output of the sample and hold card is 0 to -10 volts to encompass overscale and underscale input data levels. During the analog-to-digital conversion of each input channel, the input to card 9 is isolated by a level shift of the sample command received from A/D timing card 7. At this time the output level is maintained by the charge on the storage device. This feature is provided to prevent changes in the data value during the conversion process.

The analog-to-digital conversion is accomplished on cards 7 and 8 by a process of successive approximations. During the conversion period, the data value for the channel being processed is compared on the ladder and switches card with the analog equivalents of a series of "trial" words produced by the analog-to-digital timing card. The first trial word is a half-scale data word (MSB = 1, bits 2 through 10 = 0). A comparator amplifier circuit on card 8 determines whether the voltage difference between the input data value and the trial word reference value is greater or less than zero volts. On the basis of this comparison the first trial bit (MSB) is either retained or discarded by the analog-to-digital timing circuits. Retention of a trial bit results in the insertion of a binary ONE in an associated binary storage location on card 7, whereas discarding a trial bit causes a binary ZERO to be inserted in the storage location for that bit. Based on the results of the first comparison, the second trial word will be either a three-quarter scale value (MSB and bit 2 = 1, bits 3 through 10 = 0) or a one-quarter scale value (bit 2 = 1, MSB and bits 3 through 10 = 0).

Thus, it can be seen that with ten comparison cycles a 10-bit data word can be produced which represents the binary equivalent of the input data value.

At the conclusion of the conversion period, approximately 5 microseconds, the encoded word is transferred to a 10-bit parallel data storage register and stored until initiation of analog-to digital conversion of the next input channel. The outputs of this register provide the data bit input to the output circuits and to the servo loop circuits group.

4.2.4 Synchronization Circuits Group

The synchronization circuits group is composed of frame sync recognition card 10 and channels-per-frame counters and synchronization card 12. The frame sync recognition card continuously monitors the input data signals received from PDM/PAM converter card 18. Comparator circuits on card 10 provided one of five command signals (zero-scale, half-scale, full-scale, overscale, or underscale) to represent the status of the data level for each input channel. The overscale and underscale signals are routed to the servo loop and are used to generate DC offset correction voltage for the input signal prior to attaining synchronization. A zero-scale, half-scale, or full-scale signal for a channel provides a count input to an associated five-stage shift register. The five stages for each of the three shift registers are routed to the front panel FRAME SYNC PATTERN switches. These switches each select an associated stage of one of the three shift registers and couple the logic value of the selected stage to a frame sync pattern detection gate on card 10. When the outputs from the five FRAME SYNC PATTERN switches are all logic ONE levels, the frame sync pattern detection gate generates a logic ZERO Sync Pat pulse. This pulse, which is applied to the channels-per-frame counter and synchronization card, indicates that the last five channels of the input have contained the equivalent of the programmed frame synchronization pattern.

Card 12 consists primarily of a three decade BCD counter. The counter is incremented at the channel rate by clock pulses received from the clock generator card. Before synchronization is attained, the counter may be reset by either a sync pattern comparison input from card 10 or by incrementing the counter to the channel number programmed on the front panel CHANNELS/FRAME switches. After synchronization is attained, the counter is recycled (reset) only upon detection of last channel (channel N) count. During the search, or unsynchronized, mode of operation the status of the Sync Pat input from card 10 is monitored every channel period and the unit advances to the locked, or synchronized, state whenever a frame sync pattern is detected (Sync Pat a ZERO). After advancing to the synchronized state, the frame sync pattern status indication is monitored only during the last channel time period. If during channel N time the Sync Pat input to card 10 is a logic ONE indicating that the last five channels (three for RZ inputs) did not contain the frame synchronization code an error count is generated. The synchronization circuits on card 10 revert to the search mode of operation if error counts are generated for three consecutive frames of input data.

During synchronized operations the Sync output from card 10 enables the distribution of output data from the output circuits group and enables the generation of full-scale and zero-scale correction signals by the servo loop.

When synchronization is lost the $\overline{\text{Sync}}$ output from card 10 causes the front panel FRAME SYNC indicator, A2DS4 to light. The BCD channel count generated on card 10 is also routed to ZERO REF CHAN switches, FS REF CHAN switches, and DECOM CHAN switches for use in selecting specific channels of the input data.

4.2.5 Servo Loop Circuits Group

The servo loop circuits group is composed of servo DAC card 4, servo adder card 5, and servo control card 6. The function of this circuit group is to provide coarse correction for DC offset of the input signal before synchronization is obtained and to calibrate the zero-scale and full-scale reference channels thereby establishing nominal output data limits. The calibration of the zero-scale reference channel, in effect, fine tunes the DC offset.

The Model 515 accepts input signals with a DC offset of up to ±50 percent of the peak-to-peak range of the input data. However, the DC offset must be less than ±20 percent before the frame sync recognition circuits on card 10 can detect the frame synchronization code pattern in the input data format. Reduction of the DC offset to the point at which synchronization can be obtained is a function of the DC restorer circuits located on Servo DAC card 4. The DC restorer provide coarse corrections for offset of the input signal, reducing the offset to ±10 percent, or less, of the optimum input level.

When synchronization is attained, fine correction for the offset error is provided by the zero-scale (minimum data) servo loop. The zero servo loop compares the 10-bit data word representing the zero reference channel of the input format (identified by means of the front panel ZERO REF CHAN switches) with a 10-bit minimum data reference word programmed on servo adder card 5. The difference, representing remaining offset of the minimum data level, is converted to analog form, summed with the coarse correction provided by the DC restores and routed to the input amplifier card through SERVO switch A2S3 to establish the optimum minimum data level for the input signal. The zero-scale servo loop is updated at the frame rate. The SERVO switch controls the selection of the percentage of correction made per frame for detected errors.

The full-scale servo loop compares the 10-bit data word representing the full-scale reference channel in the input format (identified by the front panel FS REF CHAN switches) with a 10-bit minimum data word programmed on card 5. The difference represents the error between the input signal level and the desired maximum data level. This difference is used to vary the full-scale reference voltage applied to the analog-to-digital conversion circuits so as to compensate for the amplitude variations of the input signal level.

The front panel servo indicators (ZERO/HIGH and LOW and FS/HIGH and LOW) light when the 10-bit data words associated with the zero reference channel or full-scale reference channel are beyond the correction range of the zero-scale and full-scale servo loops, respectively.

4.2.6 Output Circuits Group

The output circuits group is composed of decommutator card 3 and output buffers card 2. This circuit group controls the distribution of the five outputs provided by the Model 515; the 10-bit binary data words, channel rate pulses, frame rate pulses, frame sync status level, and the decommutated channel analog output.

The 10-bit binary data words generated in the analog-to-digital conversion circuit group are normally gated through the decommutator card and buffer stages on card 2 to rear panel output connector A3J1. However, if the Model 515 is not in frame synchronization, as determined by the synchronization circuit group, and is not operating in one of the three calibration modes, the binary inputs to card 3 are inhibited and the output data is driven to the all zero state. The 0° strobe pulses applied to card 3 from the clock generator are delayed and coupled through a buffer stage on card 2 to output connector A3J1 as the channel rate output pulses. In a similar manner the counter reset pulses generated at the frame rate on card 12 are delayed on card 3 and coupled to connector A3J1 as the frame rate output pulses. Delay of the channel rate and frame rate pulses is provided to allow the binary data words to stabilize on the lines before being loaded into an external device. The frame sync output from card 3 to rear panel connector A3J1 is the sync status level received from the synchronization circuits.

The decommutator card also has the capability of storing the 10-bit binary word associated with a selected channel of the input format and converting the selecting channel data to analog form. Selection of the specific channel to be decommutated is controlled by the front panel DECOM CHAN switches. The analog value associated with the decommutated channel is provided as an output at rear panel connector A3J5 and is also displayed on the front panel DECOM meter A3M3. During synchronized operation the data value for the selected channel is updated at the frame rate. If synchronization is lost the data value is held constant until synchronization is recovered.

4.2.7 Power Supply and Regulation Circuits

The primary DC operating voltages required by the Model 515 are provided by an internal power supply and regulated by circuits located on regulator card 21. The power supply, composed of transformer A1T1 and diode bridge circuits A1CR1, A1CR2, and A1CR3, provides three unregulated voltage outputs. These voltages are processed by five regulator circuits on card 21 to provide regulated outputs of +5V DC, +15V DC, +20V DC, −15V DC, and −20V DC. In addition, outputs of +12V DC and −6.2V DC are produced by zener diode regulators on card 21.

4.3 DETAILED THEORY OF OPERATION

The following paragraphs provide detailed functional description of the individual printed-wiring boards contained in the Model 515. The descriptions are presented, as far as is possible, in the signal flow sequence and each description is referenced to appropriate functional block diagrams. References are provided on each block diagram to the associated schematic diagram provided in Section 5.

4.3.1 Input Amplifier Card (Ref. Figure 4-3)

The input amplifier printed-wiring board is located in card slot 20 (J20) of the Model 515 chassis. The primary function of the circuitry contained is to condition the input data signal so as to provide signal levels compatible with other circuits of the synchronizer. The input amplifier card also contains control circuitry for front panel INPUT meter A2M1 and a precision voltage divider network which provides DC voltage levels for test and calibration of the Model 515.

The incoming data signal is applied to rear panel connector A3J4 and routed through front panel input potentiometer A2R1, POL (polarity) switch A2S4, and CALIBRATOR switch A2S1 to the input amplifier card. The Model 515 accepts PAM-NRZ, PAM-RZ, or PDM signals with data levels of from one to 30 volts peak-to-peak. Potentiometer A2R1 is manually adjusted to attenuate the peak-to-peak input data amplitude to 0.8 volts peak-to-peak. The input data may be reflected as either positive-going (normal) or negative-going (inverted) transitions from the minimum data level. The function of the POL switch is to route the attenuated input signal to the appropriate pin of card 20 so as to allow the Model 515 to process either normal or inverted input data using the same circuitry. Normal mode inputs are applied to pin 22 and inverted mode inputs are applied to pin 21.

The signal conditioning is accomplished by the circuitry composed of differential amplifiers Q1/Q2 and Q3/Q4 and level shifter network Q5 through Q8. These stages are arranged as a precision operational amplifier with a gain of 5. The 0.8 volt peak-to-peak swing of the input signal thus is amplified to a 4-volt swing from maximum data level to minimum data level which is referenced at +5 volts (+3 volts to +7 volts). For normal mode inputs (signal amplitude positive-going as data magnitude increases), the input amplifier circuitry provides a polarity inversion. Thus, a maximum data input is represented at the output by minimum level signal (+3 volts) and a minimum data input is represented by a maximum signal amplitude (+7 volts). For inverted mode inputs (data amplitude negative-going as data magnitude increases) no inversion is required.

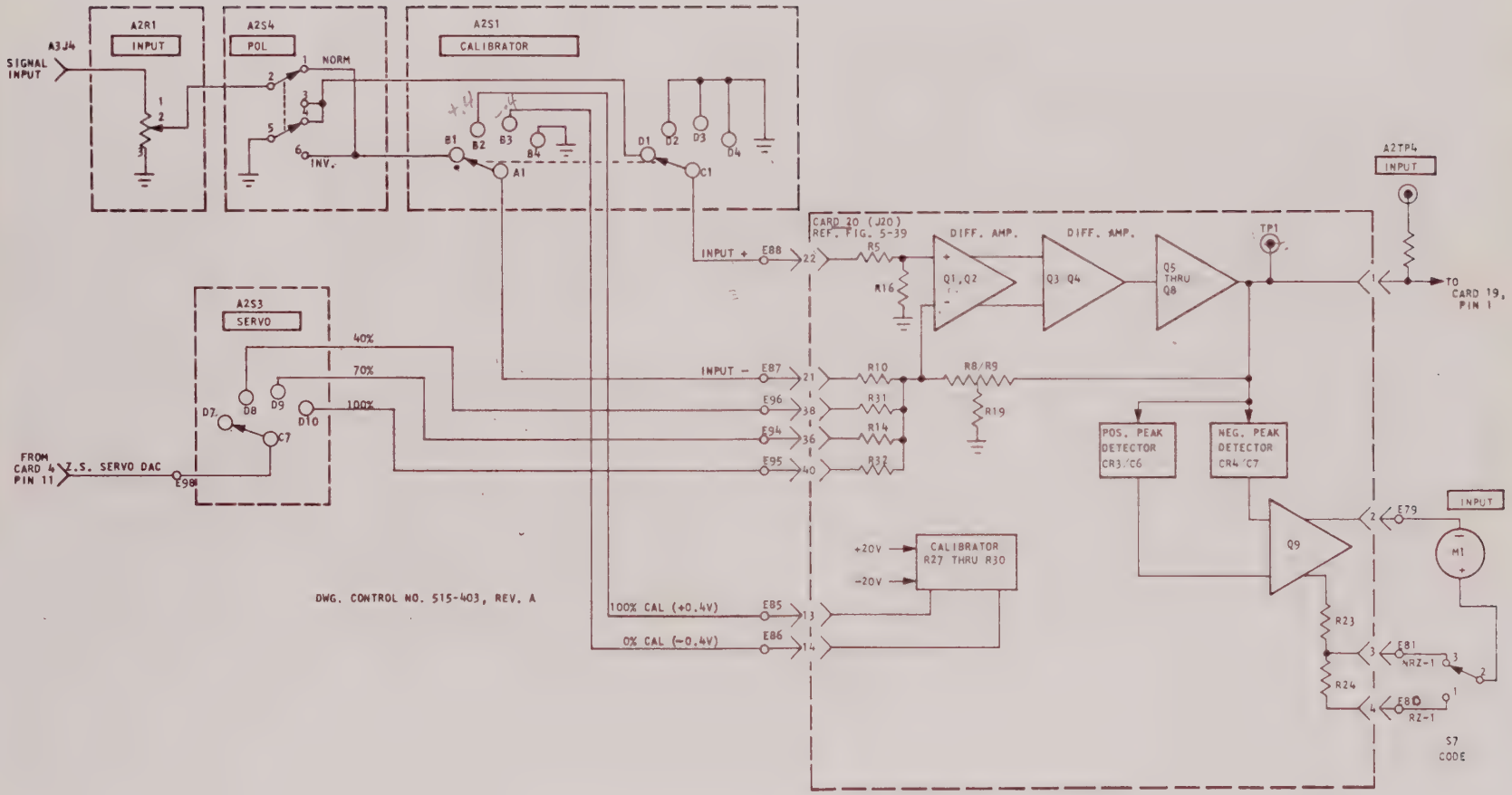


Figure 4-3. Input Amplifier (Card 20) Functional Block Diagram

NOTE

The 4-volt transition from maximum data level to minimum data level is applicable for all input data formats. However, a PAM-RZ input signal has a 50 percent duty cycle with the baseline reference being offset approximately 1-volt from the minimum data level. Thus, the overall voltage swing at pin 1 of card 20 is 5 volts (+3 volts to +8 volts) for PAM-RZ inputs. The 1-volt offset must be compensated for in the INPUT meter control circuitry as discussed in the following paragraph. However, for discussion of subsequent circuits of the Model 515, the 1-volt offset is ignored and only the maximum to minimum data amplitude swing (+3 to +7 volts) is considered.

The conditioned data signal output of card 20 is routed via pin 1 to the input filter printed-wiring board (card 19). This signal is also applied to the control circuitry for INPUT meter A2M1. This circuitry consists of a positive peak detector (CR3/C6), a negative peak detector (CR4/C7), and a high-impedance differential amplifier circuit (Q9) located on card 20 and the front panel CODE switch A2S7. Capacitor C6, which has a rapid charge time and a slow discharge time, charges through diode CR3 to the minimum data level (+7 volts) for PAM-NRZ inputs or the baseline reference (approximately +8 volts) for PAM-RZ signal. Likewise, capacitor C7 charges to the maximum data level (+3 volts) through diode CR4. Since the discharge paths for C6 and C7 are through the back resistance of diodes CR3 and CR4 as well as the high input impedance of differential amplifier Q9, the charges on the capacitors are maintained at approximately the peak levels. In the PAM-NRZ and PDM modes, the outputs from Q9 produce a current flow through resistor R23 and INPUT meter A2M1. In the PAM-RZ mode, resistor R24 is added to the series current path to compensate for the offset voltage between the minimum data level and the baseline reference. A nominal 4-volt peak-to-peak differential between the maximum data level and the minimum data level will provide a mid-scale (green band) indication on the meter. Increases or decreases in peak input signal level will cause the meter indication to shift to the upper or lower red-band areas of the scale. The INPUT meter thereby functions as a monitoring device for proper adjustment of INPUT potentiometer A2R1.

NOTE

At channel rates of less than 50 channels per second, fluctuations in the INPUT meter indication may result from infrequent changes in data. In these cases the INPUT test point on the front panel should be monitored using an oscilloscope while adjusting the INPUT potentiometer. Since this test point is actually the output of the input amplifier, the voltage should be adjusted to +7 volts and +3 volts on signal peaks.

The calibrator block shown on Figure 4-3 is a precision voltage divider network composed of resistors R27 through R30. Voltages of +0.4 volts, representing a peak minimum data level, and −0.4 volts, representing a peak maximum data level (inverted input mode levels), are tapped off the voltage divider and routed to CALIBRATOR switch A2S1. These voltages, in addition to DC ground, provide precision DC levels for test and calibration of the Model 515 at the 0%, 100%, and 50% data levels.

As stated previously, INPUT potentiometer A2R1 provides a means of calibrating the peak-to-peak input to the Model 515. However, this is only a coarse adjustment. Fine tuning is accomplished by zero-scale and full-scale servo loops which compare precision preset data values with the data values extracted from reference channels of the input format. From this comparison, zero-scale and full-scale error signals are generated. The zero-scale error signal is routed from the Servo DAC card 4 to the front panel SERVO switch A2S3. This switch provides for the selection of the per-frame correction rate for the zero-scale (minimum data level) errors. That is, in the 100% position the full error is compensated for immediately upon detection. In the 40% position the error signal applied to the input amplifier provides for 40% correction of the overall error during the frame detected, 40% of the remaining error during the second frame, and so on. In the OFF position the error signal is not used.

4.3.2 Input Filter Card (Ref. Figure 4-4)

The function of the input filter printed-wiring board, card 19, is to attenuate noise components of a PAM-NRZ signal received from the input amplifier circuit on card 20.

NOTE

If the Model 515 is processing a PAM-RZ or PDM input format, the input filter circuit must be deactivated by setting FILTER switch A2S6 to the OUT position.

The input filter is a three-pole, Bessel-type filter with a constant delay filter response characteristic. Each pole of the filter is composed of discrete RC components with the specific components selected at any given time being a function of the CHANNEL RATE selector switches. Component values are selected to provide a filter cutoff frequency equal to the programmed channel rate (10 Hz to 100 kHz). The most significant and second most significant digit switches (A2S22 and A2S23, respectively) of the CHANNEL RATE grouping of thumbwheel switches each provide a four-line, binary-coded-decimal input to control gates and driver stages on card 19. Each logic ONE level BCD input bit activates an associated transistor switching gate, thereby coupling the PAM signal through the gate and its associated resistor. Thus, any number (1 to 9) programmed as the most significant digit will activate one or more switches and the associated resistive components in each pole of the filter. The multiplier switch (A2S20) in the CHANNEL RATE grouping of switches provides a single active output (logic ONE level) for each of five positions for the switch.

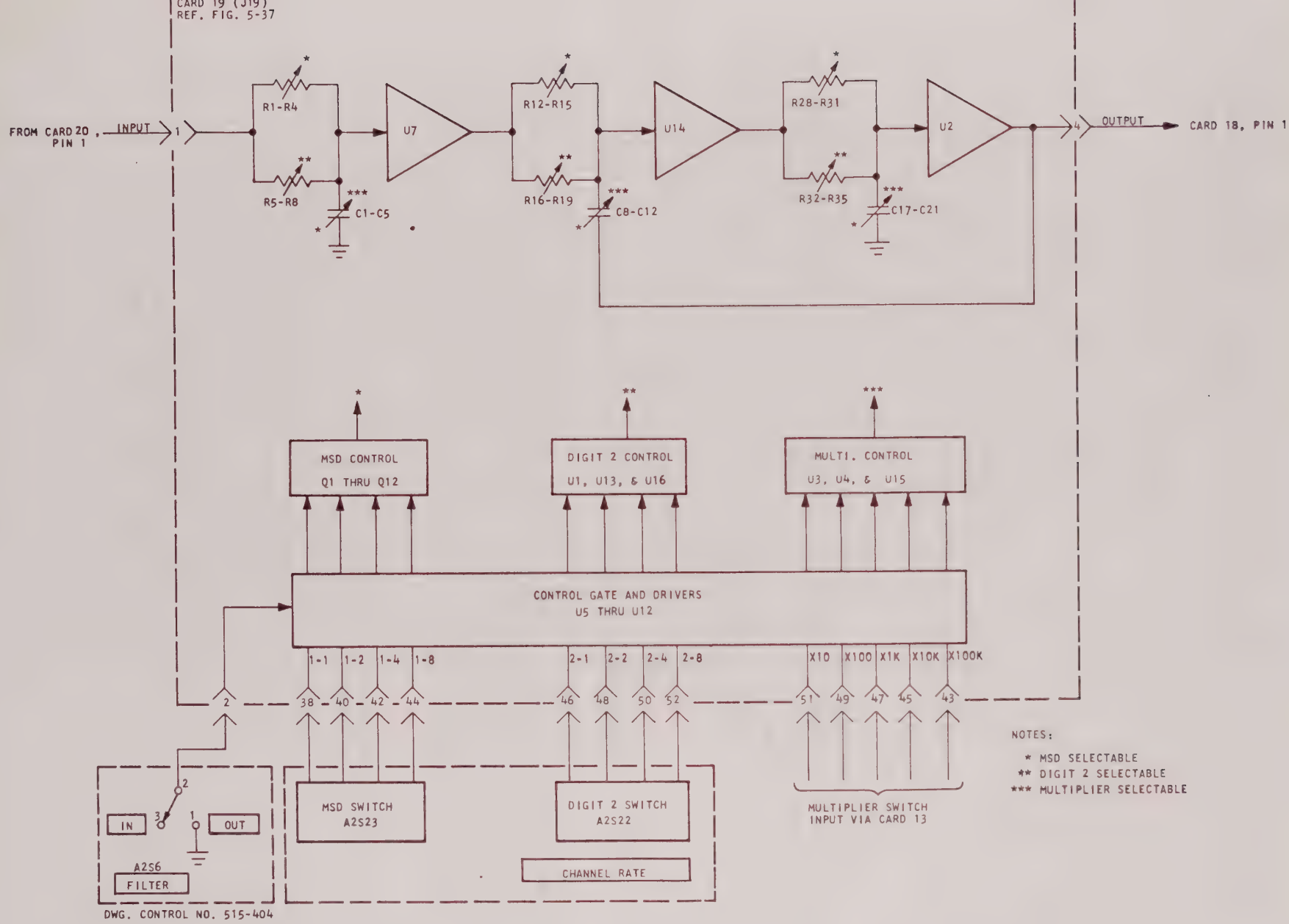


Figure 4-4. Input Filter (Card 19) Functional Block Diagram

Each position provides for selection of a specific capacitive value, associated with a range of cutoff frequencies, in each pole of the filter. The switch position - multiplication factor - channel rate relationships are as follows:

Switch Position	Multiplier	Range
1	x 10	10.0 to 99.9 CH/S
2	x 100	100.0 to 999.0 CH/S
3	x 1K	1.0 to 9.99K CH/S
4	x 10K	10.0 to 99.9K CH/S
5	x 100K	100.0 to *K CH/S

*Although the CHANNEL RATE switches may be programmed to 999.0K CHAN/S, the Model 515 specifications are binding only to 100.0K CH/S.

In order to prevent interaction between filter poles, isolation amplifiers are used between each RC network. An in-phase feedback loop is provided between the output of the third isolation amplifier stage (U2) and the input of the second isolation amplifier stage (U14). The purpose of the active feedback loop is to shape the frequency response in a manner that is not possible with only passive components. The feedback loop, in effect, varies capacity as a function of frequency in order to maintain the actual output response curve at an amplitude level as close as possible to the optimum curve.

4.3.3 PDM/PAM Converter Card (Ref. Figures 4-5 and 4-6)

The function of the PDM/PAM converter printed-wiring board, card 18, is to convert the signal characteristics of a pulse duration modulated (PDM) input to signal types required at the inputs of the analog-to-digital conversion circuit group, the phase-locked-loop circuit group, and the synchronization group. To provide the input characteristics required by each circuit group, the PDM/PAM converter card contains three functional circuits: a PDM-to-PAM converter, a differentiator, and a single pole filter.

The PDM-to-PAM converter circuit converts pulse duration coded data contained in the PDM input signal to representative analog data values as required by the analog-to-digital conversion circuit group. This circuit group is composed of a variable integrator network (R1 thru R8 and C11 thru C14), start and stop control gates Q23 and Q27 respectively, differential amplifiers U4 and U5, and an output level adjustment voltage divider network. The PDM input received from input filter card is in inverted form as shown on the waveforms diagram, Figure 4-6, and phase-shifted as described in paragraph 4.2.2. Prior to the start of each channel period, control gate Q23 is open and gate Q27 is closed by the logic level outputs from flip-flop U1. With gate Q23 open and Q27 closed, amplifier U4 functions as a voltage follower.

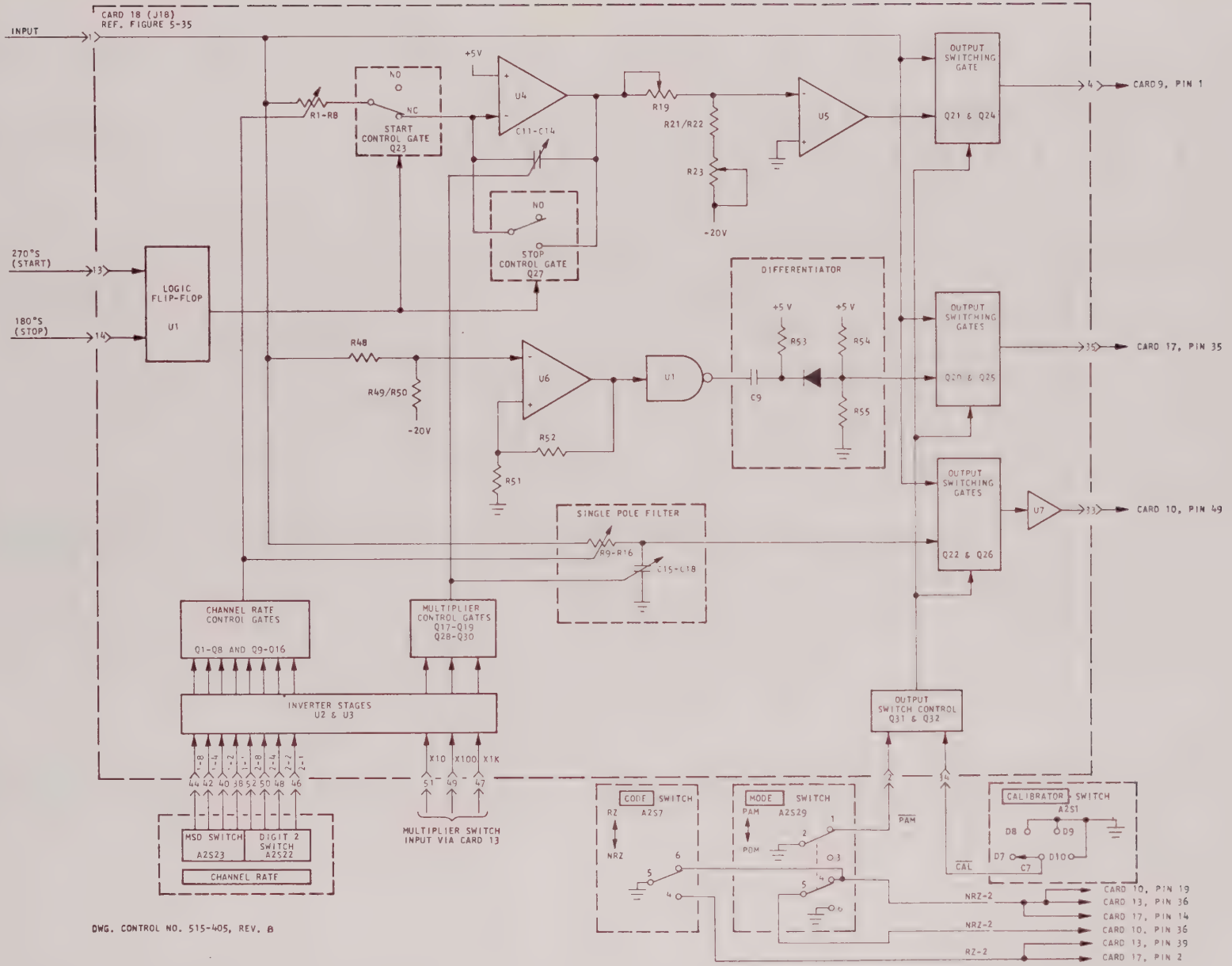


Figure 4-5. PDM/PAM Converter (Card 18) Functional Block Diagram

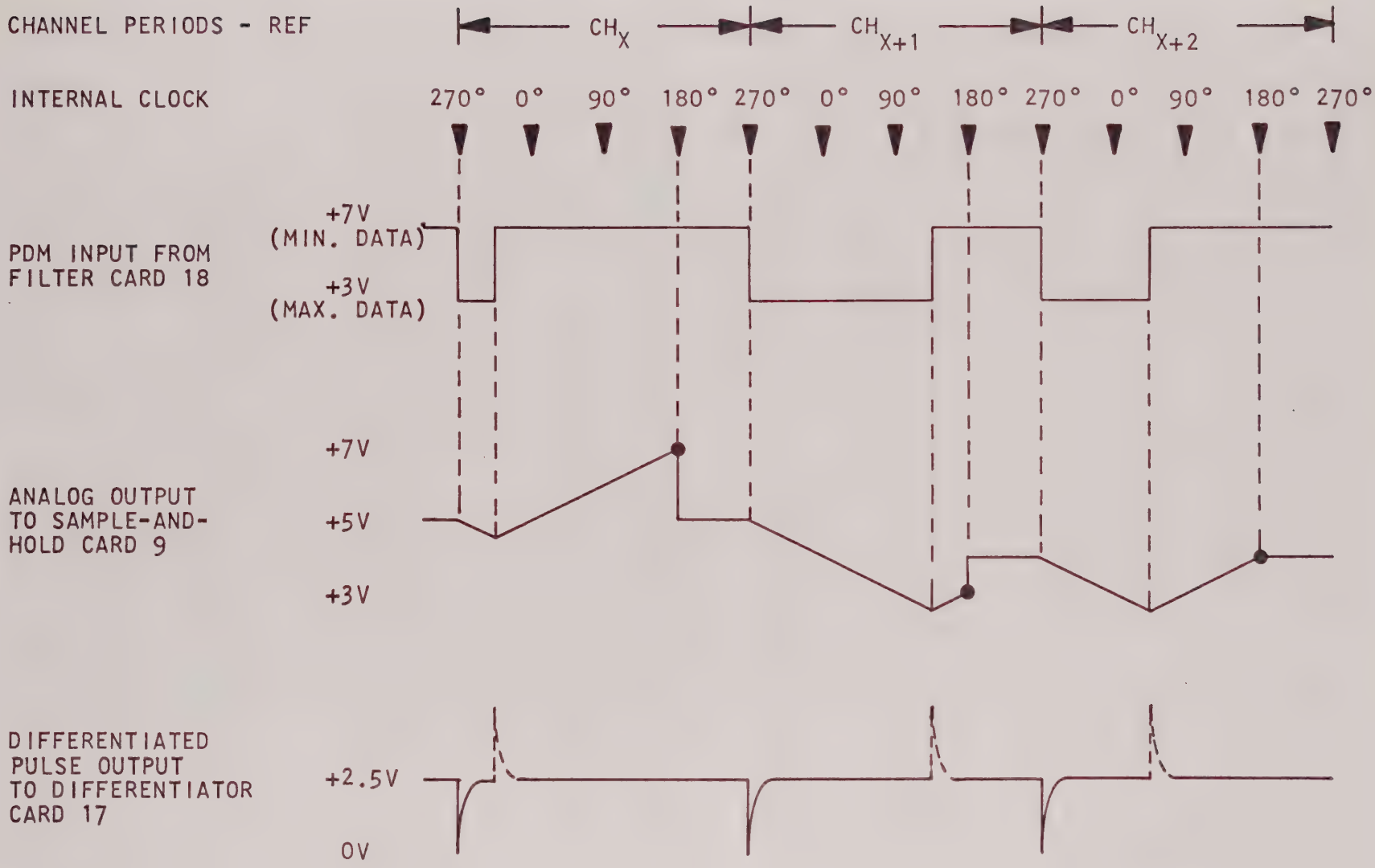


Figure 4-6. PDM/PAM Converter Card Waveforms

When the 270°S (START) pulse is received, logic flip-flop U1 changes state, closing start gate Q23 and opening stop gate Q27. As shown in Figure 4-6, the capacitive part of the integrator network discharges through U4 during the time that the PDM input is maximum (+3V). When the PDM input drops to minimum (+7V), C11-C14 charge until the 180°S (STOP) input changes the state of U1 which opens gate Q23 and closes gate Q24. Opening Q23 opens up the charge path (R1-R8 and U4) to the capacitive network C11-C14 and C11-C14 discharge through stop gate Q27. The output of U4 remains at +5V until the next 270°S (START) pulse is received, closing Q23 and opening Q27. The process is then repeated for the next channel of PDM data. The RC constants of the integrator network are varied by front-panel switches and their corresponding control gates. The CHANNEL RATE switches and control gates vary the R1-R8 resistance and the multiplier switches vary the C11-C14 capacitance.

The PDM input to the differentiator is shaped and amplified at U6, inverted at U1 and applied to the differentiator circuit consisting of C9 and R53 through R55. As shown in Figure 4-6, the differentiator output is clamped at +2.5V so that only the negative-going spike is transmitted to differentiator card 17 at the start of each channel period.

The PDM input is also routed to a single-pole filter consisting of R9-R16 and C15-C18. The filter cutoff frequency is controlled by the front-panel CHANNEL RATE and multiplier switches.

When the Model 515-03 is operating in the PAM mode, output control switch Q31, Q32 enables the PAM input (to card 18) to be routed directly through the output switching gates (Q21 and Q24, Q20 and Q25, Q22 and Q26) to the appropriate circuit cards. In the calibrate mode (CALIBRATOR switch A2S1 set to 0%, 100% or 50%), a ground (CAL) from A2S1 forces the PAM/PDM converter card into the PAM mode.

4.3.4 VCO Card (Ref. Figure 4-7)

The VCO printed-wiring board, card 14, is composed of an astable multivibrator (Q1 through Q6) and a self-starting circuit (U2 and U7). The VCO produces an output frequency in the range of 200 kHz to 2 MHz which is two times the maximum input signal range programmable on the front panel switches.

NOTE

Although the Model 515 is programmable for input signals of up to 999 K/CHAN the unit is only covered by specifications for signals up to 100 K/CH.

The specific frequency of the multivibrator oscillations is controlled by tunable resistors in the RC networks and the correction voltage input applied to pin 22 from the loop filter card. Selection of individual resistors in the RC timing networks is a function of the three digit number programmed on the front panel CHANNEL RATE switches. Each combination of digits, 100 through 999,

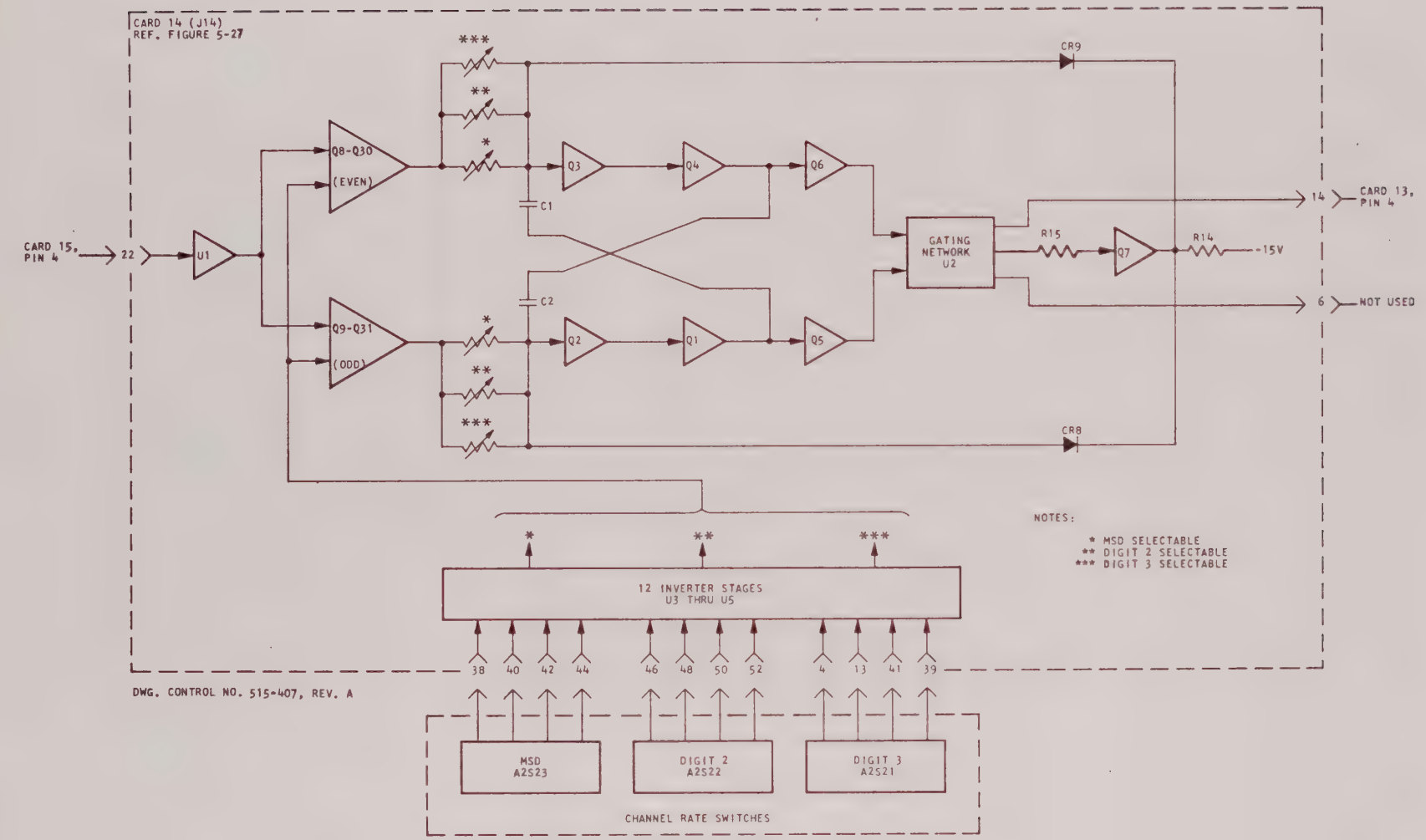


Figure 4-7. VCO (Card 14) Functional Block Diagram

activates one or more paths through the transistor switches (Q8 through Q31) with each path enabling an associated resistor. The reference level for the RC timing networks is the output of voltage follower circuit U1. When the input data signal and the internal timing pulses produced by the clock generator (card 13) are in phase, the output of U1 is a 0-volt level. Thus, a correction voltage produced by the loop filter card from a detected phase difference increases or decreases the reference voltage of the RC timing network and thereby allows the VCO to achieve and maintain synchronization with the input data signal. Since the capacitive components, C1 and C2, in the RC timing networks are of fixed values, the VCO produces the same range of frequencies (200 kHz to 2 MHz) for each frequency band selectable by the multiplier control of the CHANNEL RATE switches.

The complementary output from each half of the oscillator is coupled through an emitter-follower stage (Q5 and Q6) and applied to gating network U2. The gating network performs the dual functions of shaping the output waveform and of insuring that oscillations start following application of power to the Model 515. When power is applied to the unit it is possible that the VCO output stages (Q1 and Q4) may both be in a saturated condition (0-volts output) thereby inhibiting oscillations. This condition is detected by gating circuit U2 which reverse biases normally conducting transistor stage Q7. When Q7 is cut off the negative-going transition at the junction of resistors R14 and R15 is coupled through diodes CR8 and CR9 to reverse bias multivibrator stages Q2 and Q3, respectively. The resultant positive transitions at the outputs of Q2 and Q3 are coupled through the follower stages Q1 and Q4, respectively, thereby initiating a change in the power turn-on conditions of these stages. However, the inherent characteristics of individual components in each half of the multivibrator allow one half to become initially dominant of the other and thus start the oscillating action.

Complementary square-wave outputs from the gating circuit are applied to pins 6 and 14 of the VCO card. However, only the in-phase output (pin 14) which is routed to the clock generator card is used.

4.3.5 Clock Generator Card (Ref. Figure 4-8)

The function of the clock generator printed-wiring board, card 13, is to produce the internal timing signals used to synchronize operation of the Model 515 with the input data signal. The 200 kHz to 2 MHz VCO output signal, determined by the settings of the CHANNEL RATE digit switches, is applied to pin 4 of the clock generator card and routed to the input gating circuit (U2 and U3) and to the divider network (U8 through U11). The divider network is composed of four decade counters which provide sequential divisions by 10 of the VCO frequency. For example, if the three digit number programmed on the CHANNEL RATE switches were 123 the VCO would be operating at 246 kHz. This signal would be applied directly to the input gating circuit and also would be processed by the divider network to provide signals of 24.6 kHz, 2.46 kHz, 246 Hz, and 24.6 Hz to the input gates.

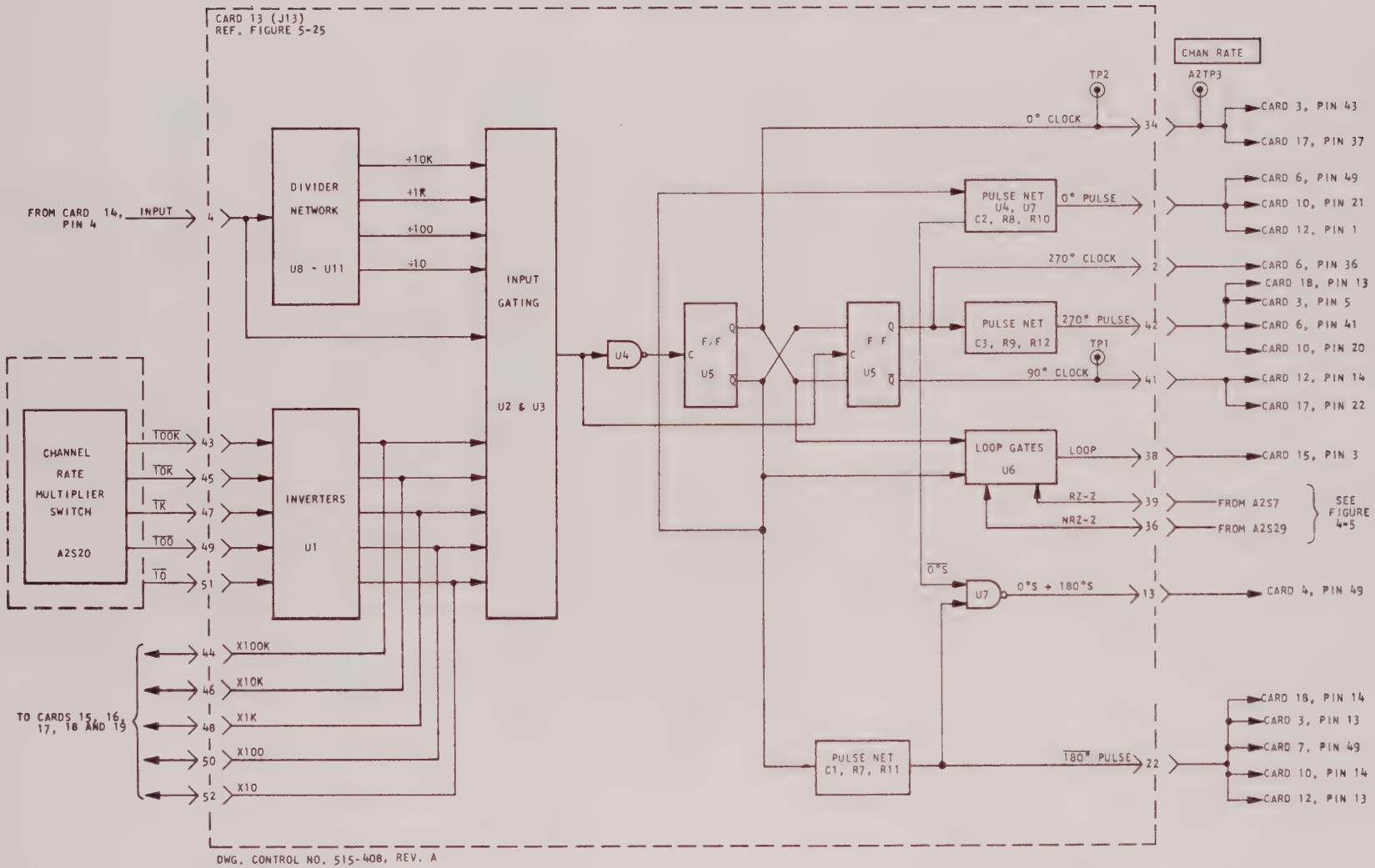


Figure 4-8. Clock Generator (Card 13) Functional Block Diagram

The CHANNEL RATE multiplier switch, A2S20, provides a logic ZERO input to card 13 for the frequency band selected and a logic ONE input for each of the four non-selected bands. Inverter stages on integrated circuit U1 invert the input levels and route these signals to the input gates. The frequency signal associated with the input gate enabled by the setting of the multiplier switch is thus routed to the pulse generation circuits. The five control signal outputs from inverters U1 (x 10, x 100, x 1K, x 10K, and x 100K) are also routed from card 13 to cards 15, 16, 17, 18, and 19.

The pulse generation circuits consists of inverter U4, flip-flops U5, loop gates U6, and the pulse forming networks for 0°, 180°, and 270° pulses. The frequency of the square-wave signal applied to the flip-flop stages is two times the rate of the input signal applied to the Model 515. Each negative transition of the square-wave signal triggers flip-flop U5 and each positive transition is inverted by U4 to trigger the second flip-flop U5. By using the outputs of both of the flip-flop stages, four timing signals are produced. Each of the four square-wave outputs is at the frequency of the input channel rate and the individual output provides timing relationships, with respect to the input signal of 0°, 90°, 180°, and 270°.

The 0°, 180°, and 270° square-wave signals are also applied to pulse forming networks. The 0° pulse network produces a positive-going, 150 nanosecond pulse for each negative transition of the 0° square wave. The 180° pulse network produces a 60 nanosecond, negative-going pulse for each negative transition of the 180° square wave and the 270° pulse network produces a 60 nanosecond positive-going pulse for each negative transition of the 270° square wave. The 0° strobe pulses and 180° strobe pulses are OR'ed to provide a composite $0^{\circ}S$ and $180^{\circ}S$ pulse train input to the DC restorer circuit on servo DAC card 4.

The loop gates circuit, U6, routes the 0° square-wave signal to the loop filter circuit, card 15, during PAM-NRZ or PDM operation and routes the 180° square-wave signal to card 15 during PAM-RZ operation.

4.3.6 Differentiator Card (Ref. Figure 4-9)

The differentiator printed-wiring board, card 17, contains three functional circuit groups: a differentiator circuit, decimal point decoder circuit, and channel synchronization detector circuit. The function of the differentiator circuit is to detect data level transitions in the input signal and to produce an output pulse for each transition of ±20 percent or greater between adjacent data levels. These pulses, which are coincident with channel transition time, are routed to the monostable printed-wiring board (card 16), and are used as the triggers for system timing pulse generation.

PDM/PAM converter card 18 provides a negative-going differentiated pulse to card 17 at the start of each channel period when operating in the PDM mode. In this mode, the function of the differentiator circuit is to establish the reference level and polarity of the pulses routed to the monostable card. The following paragraphs are primarily concerned with the generation of the monostable input pulses from PAM coded input data.

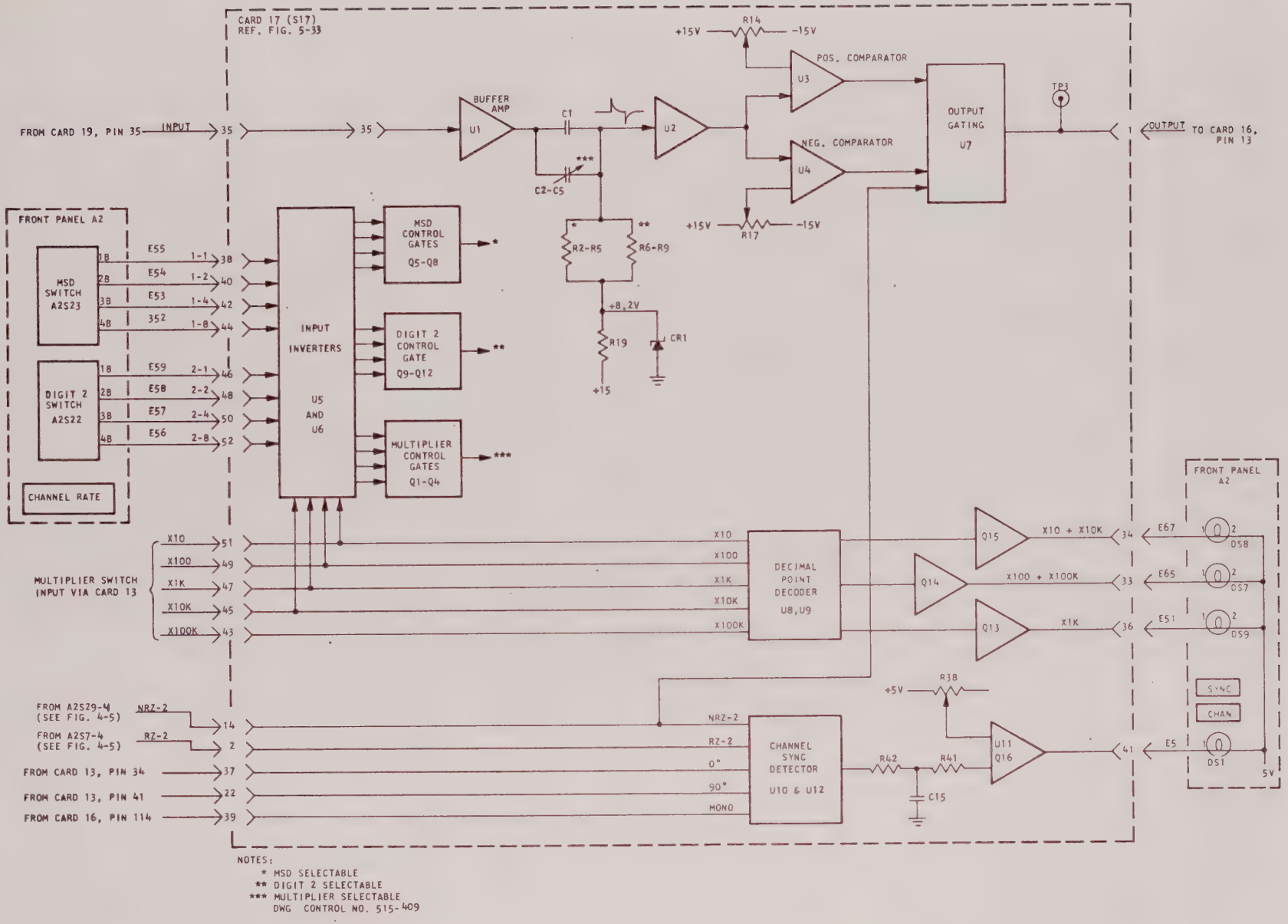


Figure 4-9. Differentiator (Card 17) Functional Block Diagram

Although the end results are similar for both PAM-NRZ and PAM-RZ inputs, the manner in which the output pulses are derived varies slightly. In order to facilitate understanding of the differences, each input type is discussed separately with reference to individual waveform diagrams.

The filtered PAM-NRZ output from card 19 is applied to pin 35 of the differentiator printed-wiring board and coupled through buffer amplifier U1 to the differentiation network composed of capacitors C1 through C5 and resistors R2 through R9. The individual capacitive and resistive components used at any given time is a function of the front panel CHANNEL RATE switches. Component values are selected so as to provide a time constant for the differentiator network of approximately six percent of the channel period for the programmed channel rate. The differentiator is referenced at approximately +8.2 volts by means of zener diode CR1. Thus, each transition of the input signal is differentiated, referenced to +8.2 volts, and applied to buffer amplifier U2. (See Figure 4-10.) The output of amplifier U2 preserves the input waveforms but shifts the reference level to approximately 0 volts. The resultant output is applied to positive and negative comparators U3 and U4, respectively. Positive comparator U3 compares positive-going transitions with a DC level (approximately +0.5 volts) representing 20 percent of peak deviation. When the positive-going differentiated pulse exceeds the reference level the comparator is triggered and provides a logic ZERO output pulse. This pulse remains in the ZERO state as long as the amplitude of the input pulse is greater than the reference level. In a like manner comparator U4 produces a logic ZERO pulse each time a negative-going differentiated pulse exceeds 20 percent of maximum negative-going deviation (approximately −0.5 volts). When operating in the PAM-NRZ mode, a logic ONE NRZ-2 level enables the outputs of both comparators through the output gating logic contained on integrated circuit module U7. Thus, a positive-going trigger pulse is routed to the monostable circuit, card 16, for each negative-going pulse output from the positive or negative comparators.

Operation of the differentiator circuit with PAM-RZ inputs is functionally the same as that discussed above for PAM-NRZ inputs except for the number of individual output pulses generated. The RZ code input data pulses have both a negative-going and a positive-going transition during each channel period. (See Figure 4-11.) Also, since the baseline reference voltage is approximately 20 percent greater than the minimum data level, an output pulse may be generated for each channel period. As shown in Figure 4-11, both transitions of the PAM-RZ input channel period are differentiated and processed by the appropriate comparator. However, during PAM-RZ operation the NRZ-2 input to the output gating logic is a logic ZERO inhibit level. Thus, only the output pulses from negative comparator, corresponding to the leading edges of the input pulses, are gated to the monostable circuit.

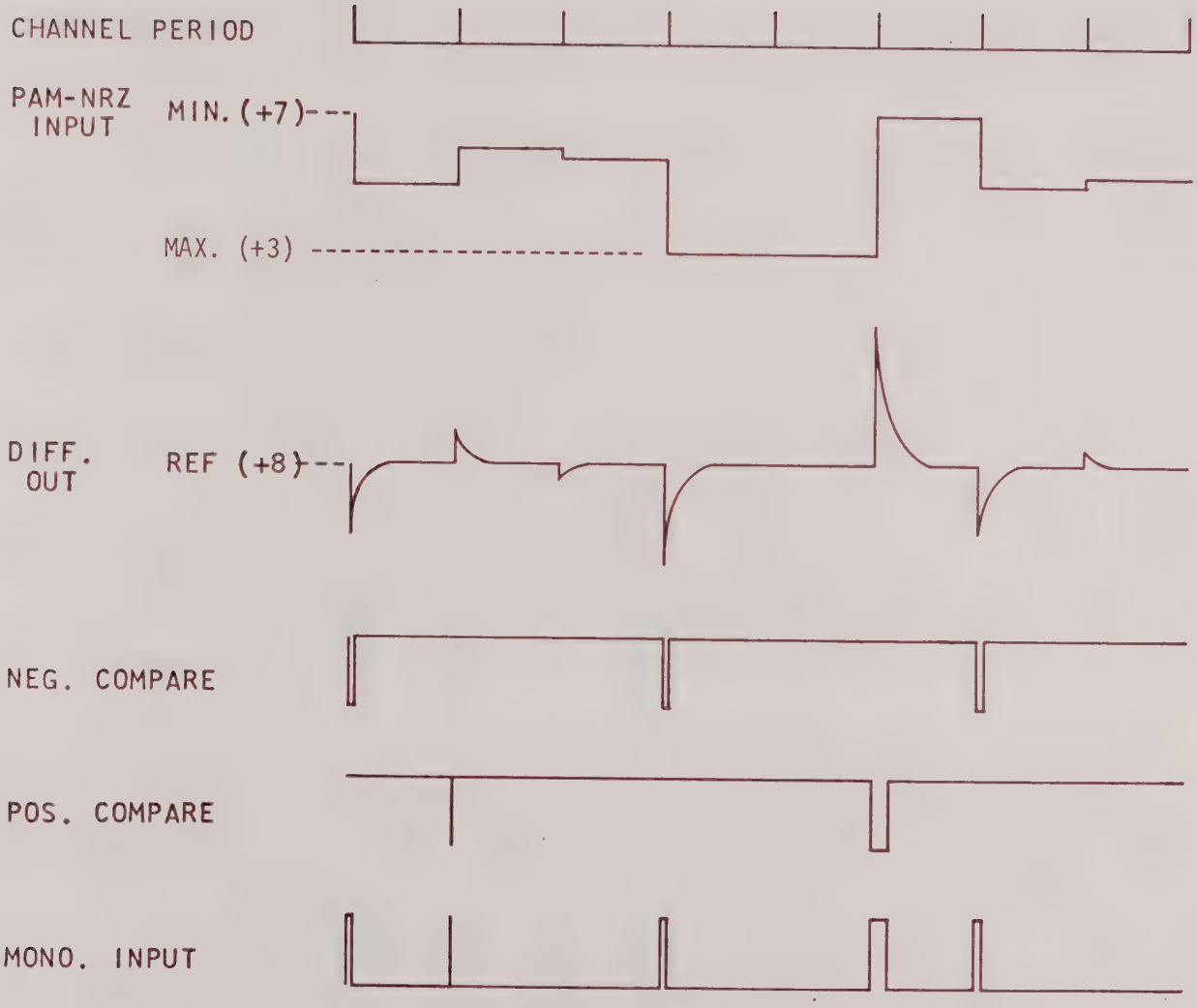


Figure 4-10. Differentiator Circuit Waveform with PAM-NRZ Inputs

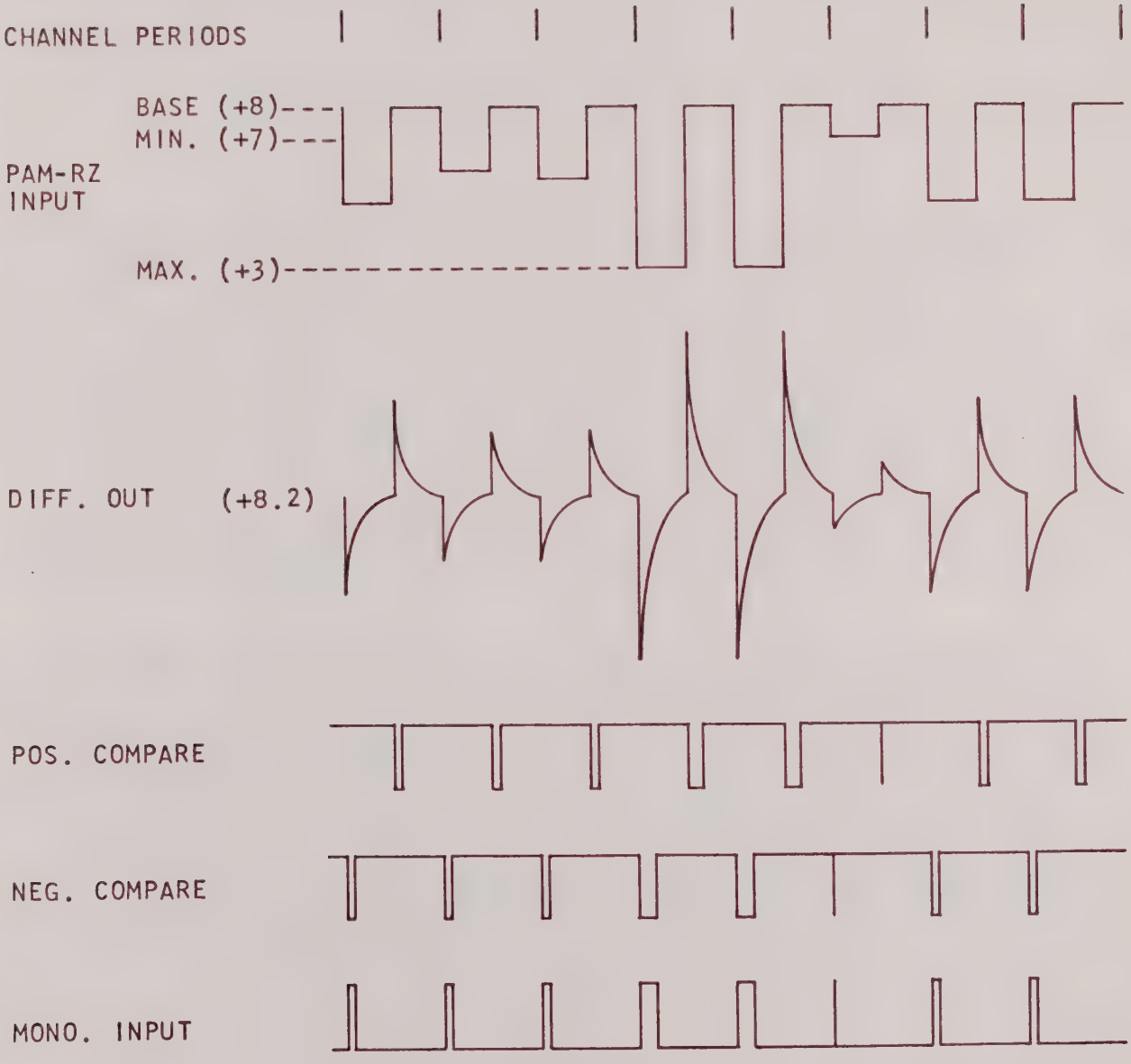


Figure 4-11. Differentiator Circuit Waveforms with PAM-RZ Inputs

The decimal point decoder circuit monitors the five output lines from the CHANNEL RATE multiplier switch, A2S20, and provides a DC return for the appropriate CHANNEL RATE decimal point indicator. The association of channel rates, multiplier input, and activated indicator is as follows:

Programmed Channel Rate			Multiplier	Indicator Lite
10.0 CH/S	to	99.9 CH/S	x 10	DS8
100. CH/S	to	999. CH/S	x 100	DS7
1.0K CH/S	to	9.99K CH/S	x 1K	DS9
10.0K CH/S	to	99.9K CH/S	x 10K	DS8
100.K CH/S	to	---	x 100K	DS7

The channel sync detection circuit compares the phase relationship of output pulses produced by the monostable card (data transitions) with timing pulses produced by the clock generator. When the input signal to the Model 515 is in PAM-RZ form the detector compares the monostable pulses with the 90° clock pulses. When the input is in PAM-NRZ or PDM form the 90° pulses are inverted to provide the equivalent of 270° pulses and then compared with the data transition pulses. If the pulse periods are synchronized, the output of the phase comparator is clamped at a logic ZERO level. Thus, no charge is applied to capacitor C15 and the input to the (+) terminal of operational amplifier U11 remains negative with respect to the (-) input (approximately +2.5 volts) established by potentiometer R38. The resultant output of U11 (approximately 0 volts) reverse biases transistor switch Q16 thereby opening the DC return path for CHANNEL SYNC indicator A2DS1.

When the phase of the compared signals is offset or if the input data pulses are missing, the comparator produces logic ONE pulses with pulse durations equivalent to the period of the polarity difference between the two signals. The positive pulses from the comparator cause capacitor C15 to charge toward the logic ONE level (+5 volts). When the charge on C15 exceeds the reference level at the (-) terminal of U11, the output of U11 is switched to a logic ONE level causing Q16 to turn on. With Q16 conducting, a return path for the +5-volt indicator power is provided through the transistor causing indicator A2DS1 to light. Potentiometer R38 is adjusted so that during PAM-NRZ operation with a 64-channel frame containing only a frame sync pattern (no data transition) the CHANNEL SYNC indicator will just remain extinguished.

4.3.7 Monostable Card (Ref. Figure 4-12)

The function of the monostable printed-wiring board, card 16, is to produce a logic ZERO output pulse for each positive-going input trigger received from the differentiator card. The output pulse width is varied as a function of the programmed channel rate. The pulse duration is selected to be approximately one-half the duration of an input channel period.

In the quiescent state transistor stages Q1, Q2, and Q5 are biased off and stages Q3, Q4, and Q6 are conducting. The capacitor (C1, C2, C5, C7, or C8) of the activated RC combination is charged to +15 volts. Each positive pulse applied to pin 13 from the differentiator card is coupled through I-C input buffer stages, U2, and drives Q5 into conduction. The resultant negative-going pulse output from Q5 is coupled through follower Q1 and the selected capacitor and is applied to Q3, causing Q3 to cut off. When Q3 turns off diode CR7 is forward biased and the positive-going output pulse is coupled to transistor stages Q2 and Q6. The positive pulse input to Q2 causes this stage to conduct which, in turn, holds transistor Q1 in the conducting state. The circuit is held in this condition to permit the selected capacitor to discharge. The discharge rate, determined by the original charge on the capacitor and the selected resistance, establishes the output pulse width. When the selected capacitor has discharged, Q3 turns on causing Q4 to turn on also which then turns off Q2 and Q1. The selected capacitor is then recharged to the +15 volt level through resistor R2.

The pulse output of transistor stage Q4 is coupled through follower Q6 and logic inverter U2 to output pin 14. Thus, each positive pulse transition at the input produces a negative-going output pulse, with a pulse width of approximately one-half the input channel width, which is routed to the differentiator card and to the loop filter, card 15.

4.3.8 Loop Filter Card (Ref. Figure 4-13)

The loop filter printed-wiring board, card 15, is composed primarily of a phase detector circuit, a two-pole filter, and a loop amplifier. The function of this card is to compare the phase relationship of the monostable output signal, which identifies the channel periods of the input data, with either the 0° clock when processing PAM-NRZ or PDM input data or with the 180° clock when processing PAM-RZ input data. Based on this comparison, the loop filter generates a correction voltage which is routed to the VCO to maintain a 90° phase difference between the input signals.

The phase detector circuit, U17 and U18, performs an exclusive OR function to determine the phase relationship between the compared signals. A phase difference of 90° is recognized by the phase detector as a zero phase error. If a zero phase error condition exists, the output of the phase detector is a symmetrical square wave at a frequency of two times the input channel rate. This signal is filtered and amplified by loop amplifier U10 to provide a zero-correction voltage for the VCO.

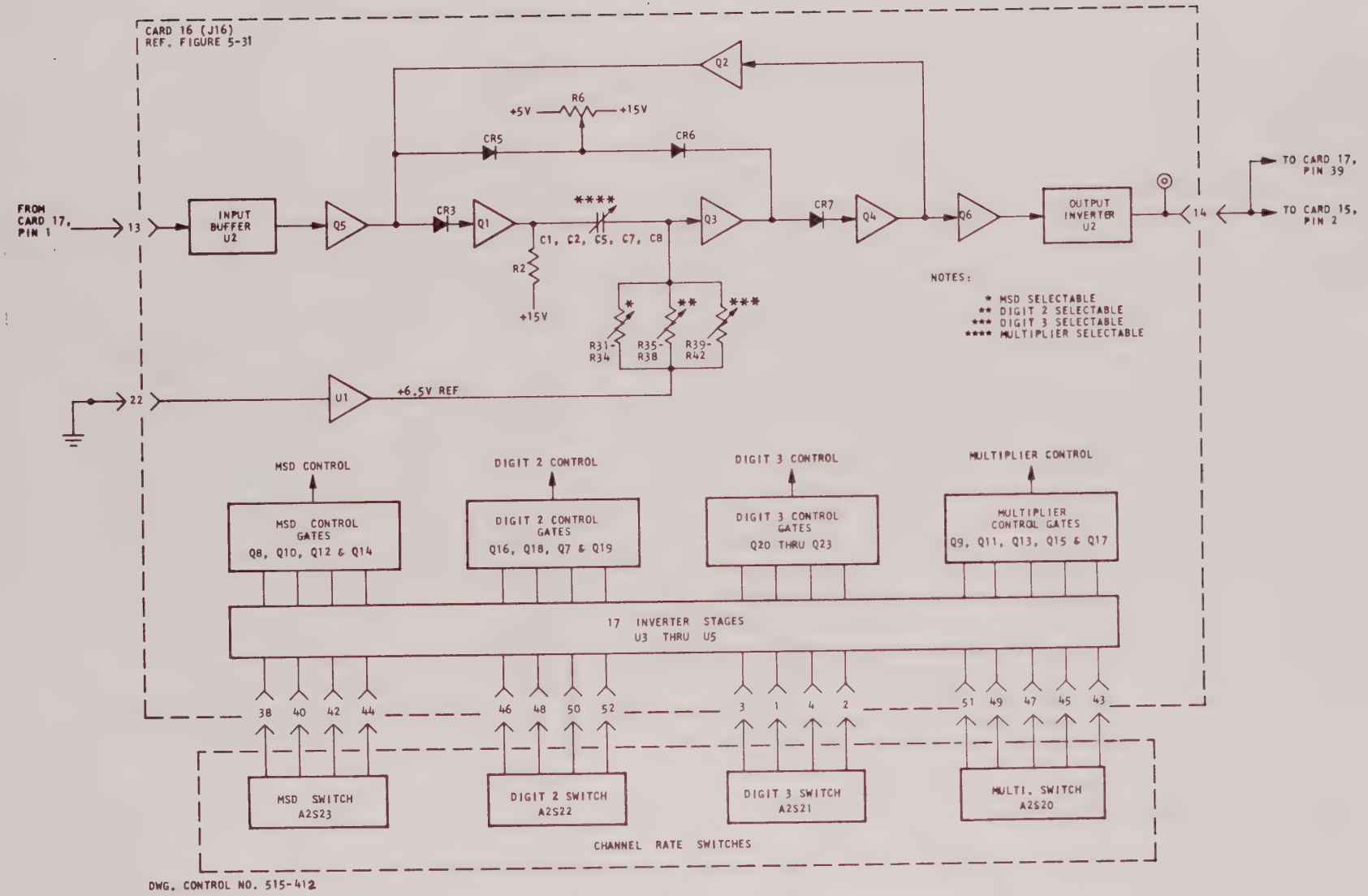


Figure 4-12. Monostable (Card 16) Functional Block Diagram

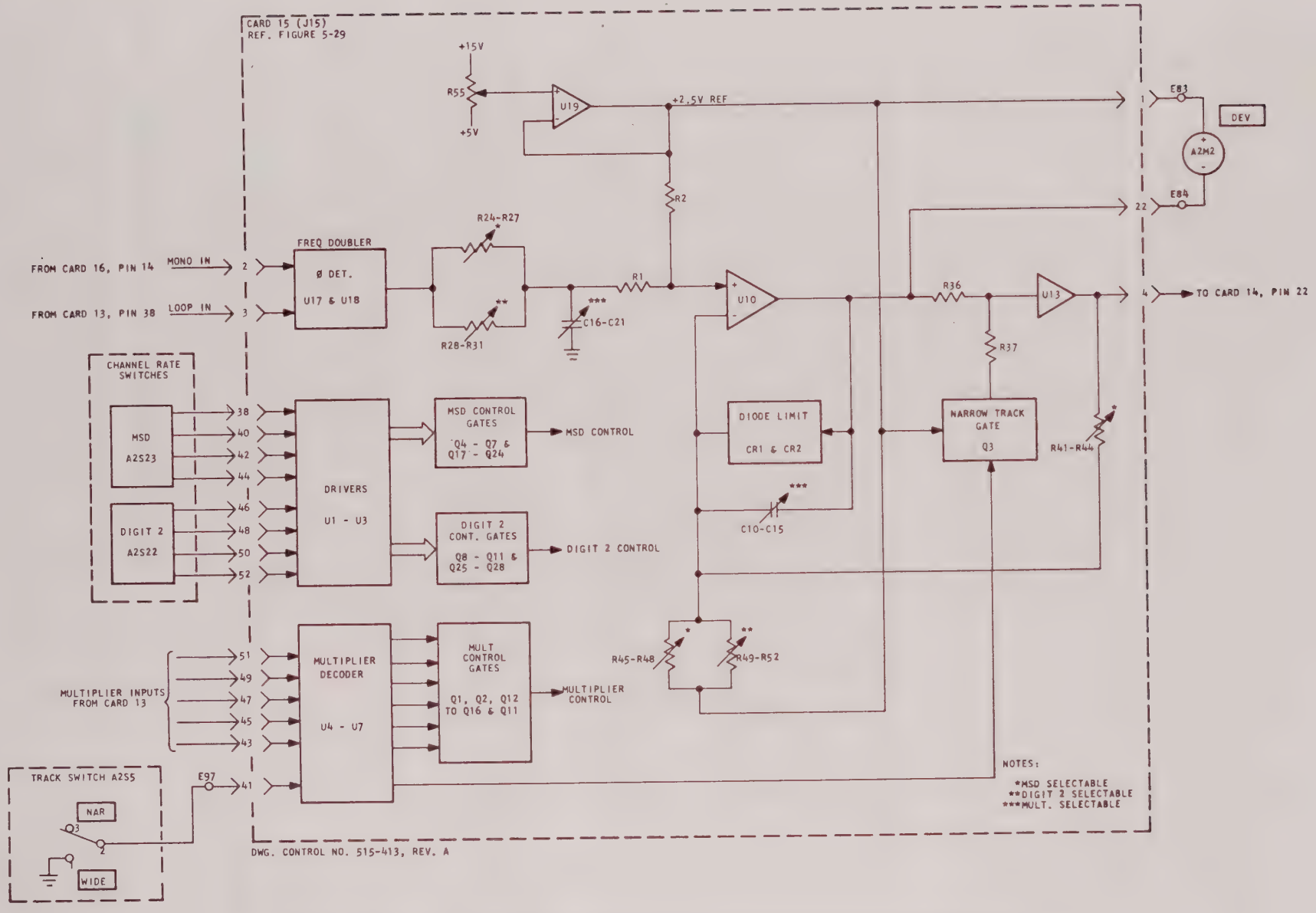


Figure 4-13. Loop Filter (Card 15) Functional Block Diagram

If the frequency of either the input channel rate or the VCO is deviated, the phase detector recognizes the shifting relationship of the input signals and the resultant output becomes nonsymmetrical. The DC component of this nonsymmetrical square wave when filtered by the frequency selectable components of the first filter pole (R24 through R31 and C16 through C21) represents the change in the phase relationship. The polarity of the filtered signal represents the direction of change. The DC component is applied to the (+) input of loop amplifier U10, amplified, filtered by the second filter pole composed of frequency selectable components R45 through R52 and C10 through C15, and coupled through buffer amplifier U13 to the VCO. This voltage changes the VCO frequency by an amount equal to the deviation detected in the phase detector. The overall action is to cause the VCO to operate at the exact frequency of the input signal and to bear a fixed phase relationship to it.

The diode limiter network, CR1 and CR2, in the feedback loop of amplifier U10 limits the peak deviation of the output from U10 to ±1 volt with the front panel TRACK switch, A2S5, in the WIDE position. This provides a correction range of ±10 percent of the VCO programmed operating frequency. Also, with the switch A2S5 in the WIDE position the selected capacitive components in the filter poles limit the filter response to the rate of phase deviation provided by the phase detector at 3 percent of the programmed channel rate. When the TRACK switch is placed in the NAR position transistor gate Q3 is turned on. This inserts a 10:1 attenuation (R37) in the feedback loop of the loop amplifier thereby limiting the correction voltage at ±0.1 volt or 1 percent of the VCO operating frequency. With switch A2S5 in the NAR position the capacitive components of the loop filters are also varied by a factor of 10 resulting in a maximum rate of phase change of 0.3 percent of the channel rate.

Operational amplifier U19 functions as a voltage regulator circuit which provides a +2.5 volt reference level to the loop amplifier. Potentiometer R55 is adjusted to provide a 0-volt correction to the VCO when the monostable signal is isolated from the loop filter card.

The output of the loop amplifier is also applied to the front panel DEV meter, A2M2, which provides a relative indication of the magnitude and direction of the correction voltage coupled to the VCO.

Selection of specific values for the RC filter circuits, and selection of the appropriate feedback resistor (R41 through R44) is a function of the front panel CHANNEL RATE switches and is accomplished in the same manner as that discussed for operation of the input filter card (refer to paragraph 4.3.2).

4.3.9 Sample and Hold Card (Ref. Figure 4-14)

The sample and hold printed-wiring board, card 9, is a composite amplifier which operates in two conditions or states, sample and hold. A logic ONE level sample command at pin 37 is routed to the switching gate drivers circuit, Q18 through Q20. With a logic ONE input the switching gate drivers provide output signals which cause switching gate Q10 to open and switching gate Q8 to close.

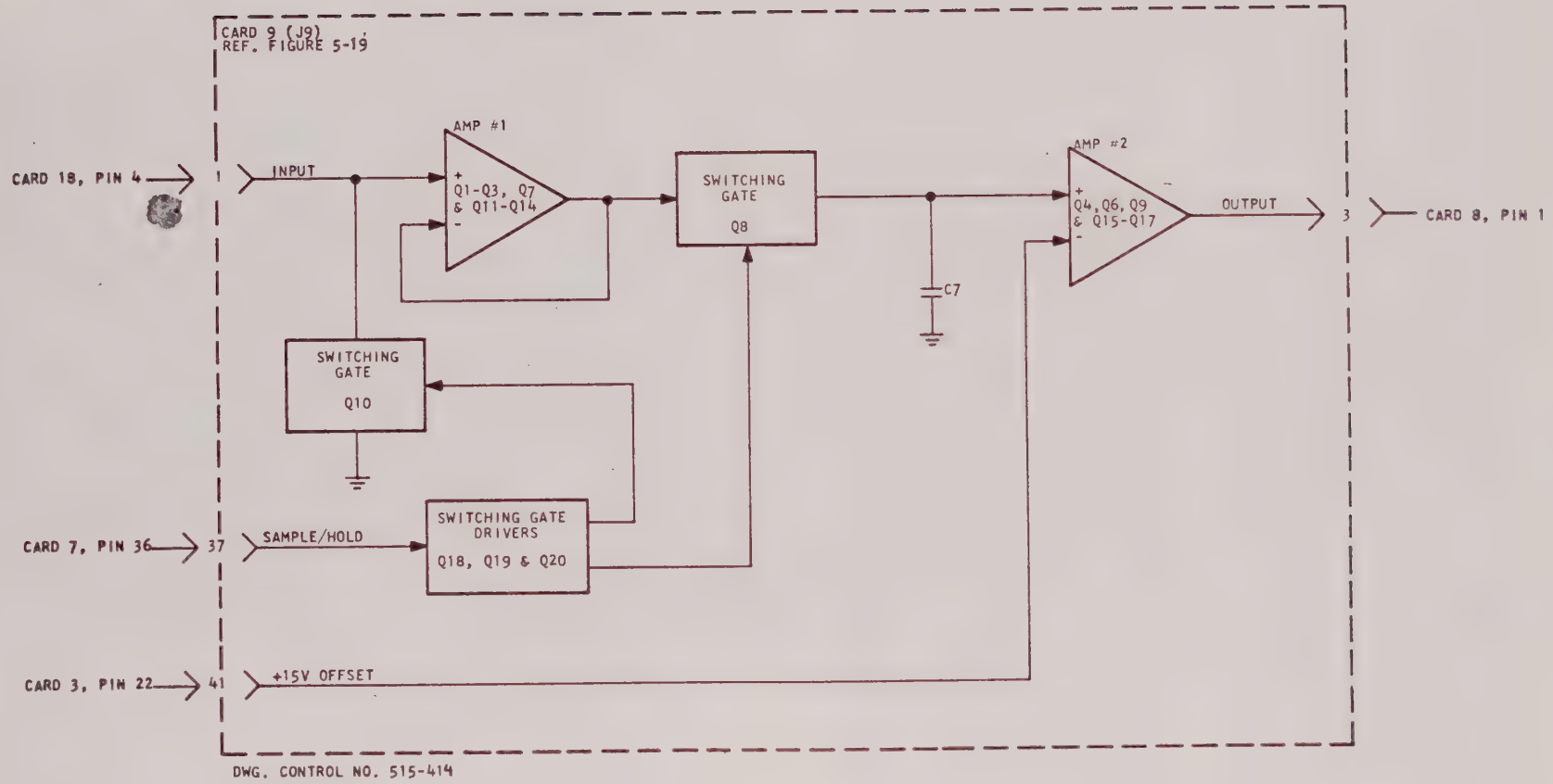


Figure 4-14. Sample and Hold (Card 9) Functional Block Diagram

This condition, called the sample state, allows the analog value for the channel being processed by the Model 515 to be applied to the first stage of the composite amplifier. The output of the first amplification stage which provides a gain of 1 is coupled through the closed switching gate, Q8, and is applied to the second amplification stage and to holding capacitor C7. The output of this stage which has a gain of +2 is the difference of the analog input value and the 15 volt offset received from decommutator card 3. Thus, the nominal voltage range of the input signal (+7.5 volts for minimum data to +2.5 volts for maximum data) is amplified and shifted to provide an output voltage range of 0 volts (minimum data) to −10 volts (maximum data).

In the sample state the holding capacitor, C7, is charged to the level of the analog value for the channel being processed. At mid-channel time (180°) the analog-to-digital timing card initiates the digitizing cycle by routing a logic ZERO hold pulse to pin 37. This pulse which is of approximately 5 microseconds duration (the period of the digitizing cycle) causes the switching gate drivers circuit to produce output levels which reverse the states of switching gates Q10 and Q8. That is, gate Q10 closes and gate Q8 opens. The first stage is thus effectively removed from the composite amplifier during the hold state. However, the holding capacitor, which charged to the analog data value for the channel during the sample condition, maintains the input to the second stage amplifier during the hold state. This function insures that the analog data for each channel is at a fixed value during the digitizing cycle.

4.3.10 Analog-to-Digital Timing Card (Ref. Figure 4-15)

The analog-to-digital timing printed-wiring board, card 7, operates in conjunction with the ladder and switches printed-wiring board, card 8, to perform the analog-to-digital conversion process. The A/D timing card provides 10-bit trial words to the ladder and switches card. This trial word is converted to an analog voltage and compared with the analog value of the input data as furnished by sample and hold card 9. Based on the results of each comparison cycle the A/D timing card establishes the binary value for a specific bit of the 10-bit output data word and determines the magnitude of the next trial word. Thus, by the process of successive approximations, an output data word is generated for each channel of the input signal by performing ten comparison operations.

At the completion of the A/D conversion period for any channel of the input signal the resultant 10-bit data word is stored in the output word storage register (U8, U16, and U22) on card 7 and the A/D timing circuits are reset (recycled) in preparation for the next conversion period. When reset, the output of the sample and hold control, U9, is a logic ONE which enables inputting of analog data to card 9. (Refer to paragraph 4.3.9.) Also, at this time, the first word comparison control, U1, and the 9-bit temporary word storage are reset. As a result, the comparison control gates provide a half-scale trial word (switches bit 1 = ONE and switches bits 2 through 10 = ZERO) to the ladder and switches card. Although this trial word is processed by the ladder and switches card the result of the first comparison cycle is not processed until the next channel conversion period is initiated by a $\overline{180^{\circ}}$ strobe pulse.

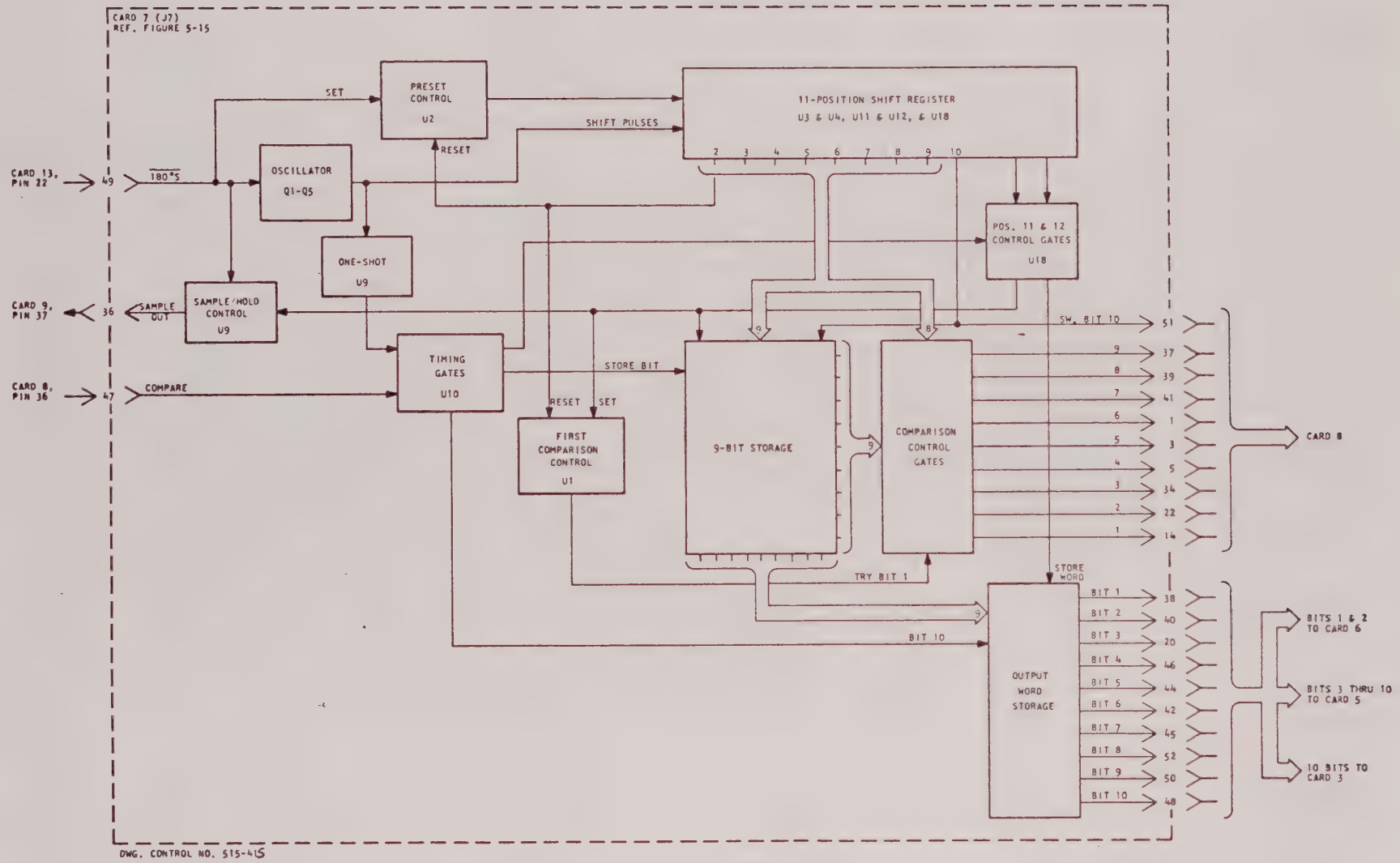


Figure 4-15. Analog-to-Digital Timing (Card 7) Functional Block Diagram

The $\overline{180^{o}S}$ pulses generated by the clock generator circuit, card 13, are coincident with the mid-data point (90°) of each channel of PAM-RZ input data or coincident with the three-quarter data point (270°) of each channel of PAM-NRZ or PDM input data. (See Figure 4-2.) The $\overline{180^{o}S}$ pulse initiates a new channel conversion period by performing the following functions:

a. Phases the 2 MHz free-running oscillator, Q1 through Q5.

b. Sets preset control flip-flop U2 to the ONE state. This flip-flop is the first stage of a 12-stage shift register. The ONE loaded into U2 is ripple shifted through stages 2 through 12 by the 2 MHz oscillator pulses to provide sequence timing for the A/D conversion process.

c. Reset the sample and hold control, U9. The resultant logic ZERO sample out level inhibits inputting of analog data to card 9.

The first positive-going oscillator pulse following the $\overline{180^{\circ}}$ strobe shifts the logic ONE level of U2 into stage 2 of the shift register. The resultant ONE level in stage 2 is inverted and routed to the reset inputs of preset control U2 and first word comparison control U1. At the same time the results of the first trial word comparison are read into the first stage of a temporary storage register. If the input data value to the ladder and switches card is greater than half scale a logic ZERO compare level is generated. This level is AND'ed in the timing gates circuit, U10, with the pulse output from one-shot circuit U9 to produce a store pulse. The store pulse causes a logic ONE to be loaded into the first stage of the 9-bit storage register. If the input data value is less than half scale the result of the first comparison is a logic ONE compare level. The logic ONE level, after inversion by U10, inhibits generation of a store pulse and the content of the first stage of the temporary storage register remains a logic ZERO.

The value of the second trial word is determined by the ONE bit in position 2 of the shift register and the content of the temporary storage register resulting from the first comparison cycle. The location of the ONE bit in the shift register forces a ONE in the corresponding bit location of the trial word. A ONE bit in the temporary storage results in a ONE in the corresponding bit location of the trial word. Thus, if the input data value were greater than the first trial word, the second trial word would be a three-quarter scale value (switches bits 1 and 2 = ONE and switches bits 3 through 10 = ZERO). If the data value were less than the first trial word, the second trial word would be a one-quarter scale binary value (switches bit 1 = ZERO, switches bit 2 = ONE, and switches bits 3 through 10 = ZERO).

The second oscillator pulse of the conversion period stores the results of the second comparison cycle and shifts the ONE bit to position 3 of the shift register at which time the third trial word is produced. Thus, the position of the ONE

bit in the shift register and the results of previous comparisons stored in the 9-bit storage register provide the successive approximations to which the input data value is compared. After nine pulses from the oscillator the ONE level is located in position 10 of the shift register, the tenth trial word is being processed by the ladder and switches card, and the 9-bit storage register contains the results of the first nine conversion cycles. The tenth oscillator pulse of the conversion period shifts the ONE level to position 11 of the shift register. At this time a store pulse is produced by position 11 control gate, U18, which loads the content of the 9-bit storage into the output word storage. The least significant bit of the output word is also stored at this time with its value being determined by the logic level of the compare signal for the tenth comparison cycle. The output word storage holds the binary value for the data channel until the conversion of the next channel of data is completed. The eleventh oscillator pulse shifts the ONE level to position 12 of the shift register which enables generation of the recycle pulse by the control gates. This pulse prepares the A/D timing circuits for the next conversion period as previously described.

4.3.11 Ladder and Switches Card (Ref. Figure 4-16)

The ladder and switches printed-wiring board, card 8, performs the arithmetic comparisons of the analog-to-digital conversion process. Each bit of the parallel 10-bit trial words received from analog-to-digital timing card 7 is applied to an associated level set control. Each level set control consists of NPN and PNP transistor stages driving complementary emitter switches in the inverse configuration. A logic ZERO at the input to a level set control provides an analog ground input to the resistive ladder network, U1, for that bit. A logic ONE input to the level set control results in the full-scale reference level established by the servo loop to be coupled to the ladder network. The ten bit level thus generated by the level set controls are binarily summed in the ladder network to provide a representative analog level.

The analog values produced by the successive approximation trial words are compared in the ladder network with the analog data level (0 to −10 volts) received from the sample and hold card and the resultant output applied to differential amplifier U2. If the difference between the compared analog values is less than zero (input data level greater than trial word value) the output from amplifier U2 is a logic ZERO level. If the input to U2 from the ladder network is greater than zero (trial word value greater than input data level) the output from U2 is a logic ONE level. The resultant output for each trial word comparison is used on the A/D timing card to generate a specific bit value in the output data word as described in paragraph 4.3.10.

4.3.12 Frame Sync Recognition Card (Ref. Figure 4-17)

The function of the frame sync recognition printed-wiring board, card 10, is to monitor the data level of each channel of the input data format in order to identify data levels which exceed the range of the Model 515 and to identify the frame sync pattern within the input format. The conditioned input data signal is applied to card 10 and routed to common inputs on six differential amplifier comparator

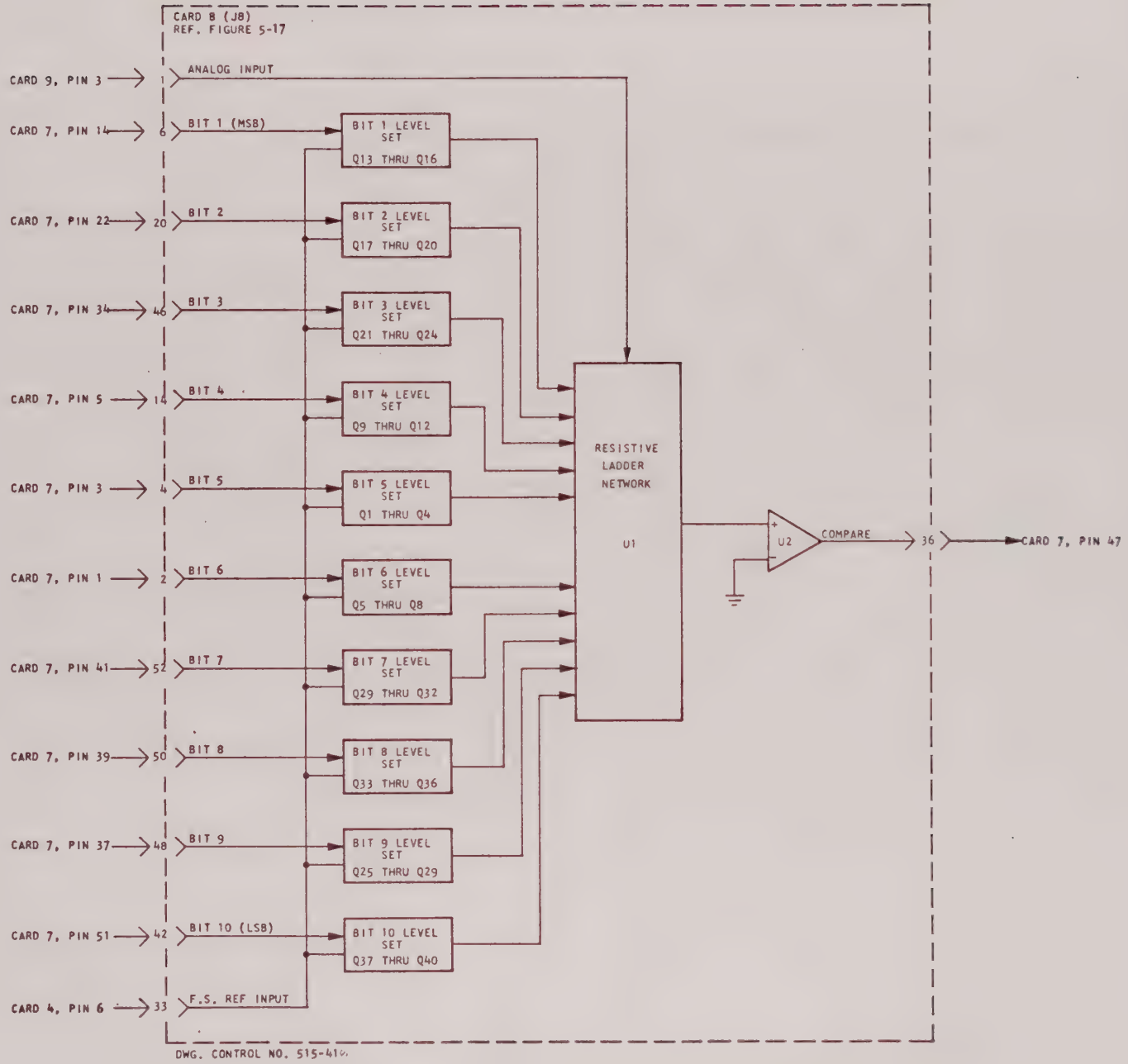
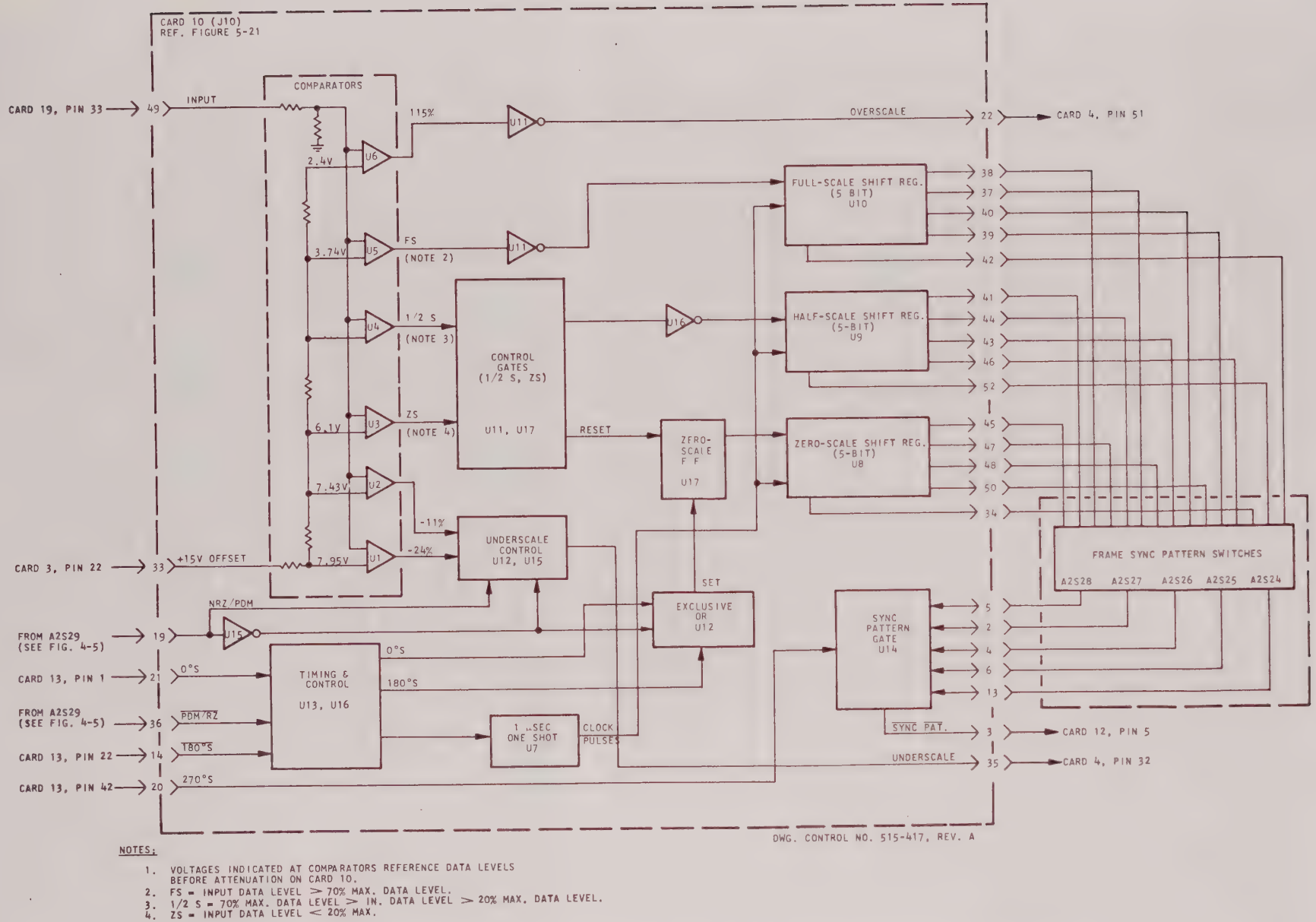


Figure 4-16. Ladder and Switches (Card 8) Functional Block Diagram



NOTES:

1. VOLTAGES INDICATED AT COMPARATORS REFERENCE DATA LEVELS BEFORE ATTENUATION ON CARD 10.
2. FS = INPUT DATA LEVEL $>$ 70% MAX. DATA LEVEL.
3. 1/2 S = 70% MAX. DATA LEVEL $>$ IN. DATA LEVEL $>$ 20% MAX. DATA LEVEL.
4. ZS = INPUT DATA LEVEL $<$ 20% MAX.

Figure 4-17. Frame Sync Recognition (Card 10) Functional Block Diagram

circuits, U1 through U6. A second input to each comparator is a DC level developed from the +15-volt offset signal applied across a voltage divider network. Thus, each comparator monitors the input data with respect to specific data levels.

As described previously, the input data from PDM/PAM converter card 18 is in an inverted configuration providing a 4-volt range (+7 volts to +3 volts) for minimum to maximum data level transitions (PAM-NRZ and PDM coded inputs) or a 5-volt range (+8 volts to +3 volts) for baseline to maximum data level transitions with PAM-RZ coded inputs. Comparator U6 is driven to the logic ZERO state whenever the input data level is less positive than 115 percent of the maximum data level (approximately +2.4 volts or less). A logic ZERO at the output of U6 is inverted by control gate U11 and routed to output pin 22 as a logic ONE overscale signal. If the input data level is more positive than −11 percent of the minimum data level (approximately +7.43 volts or greater), comparator U2 is driven to the logic ONE state. If the input data level is more positive than −24 percent of the minimum data level (approximately +7.95 volts or greater), comparator U1 is driven to the logic ONE state. The outputs of comparators U1 and U2 are gated through the underscale control circuit, U12, by the NRZ/PDM input from the front-panel MODE switch A2S29 (see Figure 4-5). When operating in the PAM-NRZ mode (PDM/NRZ = ONE), a logic ONE underscale signal is produced whenever the output of comparator U2 is a logic ONE. When operating in the PAM-RZ mode (PDM/NRZ = ZERO), a logic ONE underscale signal is generated only if the output of comparator U1 is a logic ONE. The overscale and underscale signals are routed to the servo loop where they are used to generate levels to compensate for DC offset of the input signal. (Refer to paragraph 4.3.14.)

Comparators U3, U4, and U5 are conditioned by the voltage divider network to identify zero-scale, half-scale, and full-scale data levels. The output of comparator U5 is a logic ZERO level, representing a full-scale data level, if the input signal value is less positive than 70 percent of the maximum data level (approximately +3.74 volts or less). The output of comparator U4 is a ONE whenever the input level is more positive than 70 percent of the maximum data level (approximately +3.74 volts or more). The output of comparator U3 is a logic ONE level, representing zero-scale data, whenever the input data value is more positive than 20 percent of the maximum data level (approximately +6.1 volts or more).

The output of U5 is inverted in the control gates and used as a steering input to the first stage of the full-scale register (5-bit shift register U10). The data is entered into the register by one-microsecond one-shot U7 which is triggered by the timing and control gates (U13, U16). The half-scale and zero-scale inputs from the control gates are applied to the corresponding shift register inputs in a similar manner. The steering inputs provided are such that the set input for only one first stage is enabled at a given time. Clock pulses, produced by the timing and control circuits (U7, U13, and U16), occur at the channel rate (clocked by $\overline{180°S}$) during PAM-NRZ operation and twice the channel rate (clocked by both 0°X and $\overline{180°S}$) during PAM-RZ or PDM operation. These pulses are applied to the clock inputs of the three shift registers. Thus, once

per channel (twice per channel in PAM-RZ or PDM operation), one of the first stages of the three shift registers is set to the ONE state and the other two first stages are reset to the ZERO state. The first stage of full-scale shift register U10 is set to a ONE if the input data level is greater than 70 percent of the maximum data level; the first stage of half-scale register U9 is set to a ONE if the input data level is between 20 percent and 70 percent of the maximum data level; and, the first stage of zero-scale register U8 is set to a ONE if the input data level for a channel is less than 20 percent of the maximum data level.

The full-scale, half-scale, and zero-scale inputs are shifted through the registers by the clock pulse outputs from the timing and control circuits. Thus, at any given time, five of the fifteen stages in the three shift registers contain ONE levels and only one of the common stages in the three shift registers may contain a ONE at any given time. The ONE levels, therefore, represent the approximate data content for the preceding five channels of NRZ data applied to the Model 515 or the preceding two and one-half channels of RZ or PDM input data.

NOTE

In RZ operation, the last half channel of a frame is not used for identification of the frame-sync code pattern.

The output for each shift register stage is applied to the front-panel FRAME SYNC PATTERN switches, A2S4 through A2S28, with the outputs from common shift register stages being applied to the same switch. Each switch is positioned to couple the output of one shift register stage (F, 1/2, or Z) to frame-sync pattern gate U14. When the output level for each of the selected shift register stages is a ONE, gate U14 is enabled allowing the 270° strobe pulse applied to U14 from the clock generator card to be inverted and coupled to channels per frame counter card 12 as the $\overline{\text{Sync Pat}}$ pulse.

NOTE

A fourth position, X, is provided for each of the FRAME SYNC PATTERN switches. The X or "don't care" position provides a logic ONE clamping level on the associated output line, thereby allowing identification of frame sync code patterns of less than five digits.

In PAM/NRZ or PDM, U12 allows 180°S to attempt to set flip-flop U17. If the level at U17, pin 2, is a ONE (representing zero scale), U17 is set and a ONE level is placed on D1 of U8. If U17, pin 2, is a ZERO (representing a value other than zero scale), the 180°S (which is of short duration) cannot set U17 and the input to D1 of U8 is a ZERO level. In PAM/RZ, the 180°S and 0°S are used to set U17.

4.3.13 Channels per Frame Counter Card (Ref. Figure 4-18)

The channels per frame counter printed-wiring board, card 12, is composed of an input pulse forming network, a three stage BCD counter, and a synchronization and reset control circuit. The 90° clock (square wave) signal produced by the clock generator card is applied to pin 14 on card 12 and routed to the pulse forming network composed of three NAND gates located on IC's U1 and U2, capacitor C2, and resistors R3 and R4. These components are arranged to form a gated one-shot circuit which produces a 50-nanosecond positive-going pulse for each negative transition of the 90° clock input. The negative transitions of the 50-nanosecond pulses provide the input triggers for the least significant stage of the channels counter.

The channels per frame counter is composed of units and tens BCD counting circuits, U9 and U8, respectively, and a flip-flop stage, U3, for counting the hundreds digit. Thus, the counter has a capacity of 199 although, by specification, the maximum number of channels per frame programmed at any given time will be 128. Both the true and complement value for each stage of the counter are continuously applied to ZERO REF switches A2S14 through A2S16, FS REF CHAN switches A2S11 through A2S13, DECOM CHAN switches A2S8 through A2S10, and CHANNELS/FRAME switches A2S17 through A2S19. Each set of switches performs a comparison operation which produces a logic ONE output gate whenever the counter value equals the channel number programmed on the associated set of switches. The logic ONE output gates are used to identify specific data channels required by various functional circuits of the Model 515.

When power is initially applied to the unit, the count value in the channels per frame counter is unknown. Two ways are provided for initially resetting the counter. Before synchronization is attained, any logic ZERO $\overline{\text{Sync Pat}}$ input from the frame sync recognition card will generate a counter reset pulse. Also, if the counter is incremented to its programmed count, the CHANNELS/FRAME switches provide a logic ONE channel N pulse at pin 3. This pulse is AND'ed with the 0° strobe pulse received from the clock generator card to produce a counter reset. Whenever the channels per frame counter is reset, the Model 515 advances to sync mode operation.

When synchronized the $\overline{\text{Sync Pat}}$ input from card 10 is monitored by the synchronization and reset control circuits only during channel N time. If the synchronization pattern observed at this time by the frame sync recognition card is in error ($\overline{\text{Sync Pat}}$ input a logic ONE) an input trigger is applied to a two stage sync pattern errors counter (U6). The channels per frame counter card will accept two consecutive pattern errors. However, three consecutive errors cause the synchronization circuits to revert to the search mode. The counter will therefore always recycle at the programmed number of channels per frame and recognition of the frame sync code pattern will reset the phase of the counting cycle to correspond to the input channel sequence.

The front panel FRAME SYNC indicator, A2DS1, is controlled by the synchronization status determined by synchronization and reset control circuits. When synchronization is lost, the $\overline{\text{Sync}}$ output at pin 2 is a logic ZERO level which provides a return for the unregulated lamp voltage and causes A2DS1 to light.

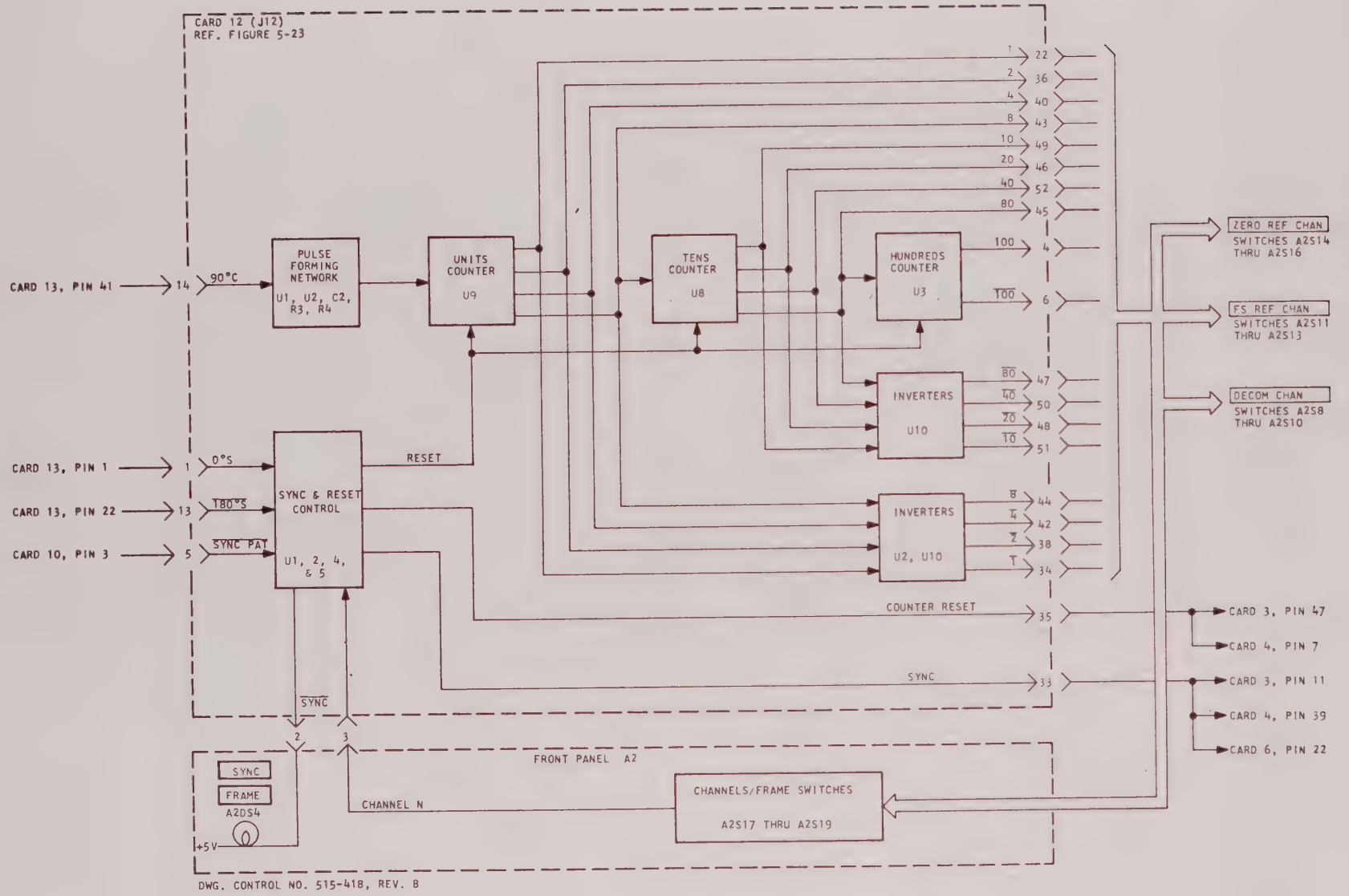


Figure 4-18. Channels per Frame Counter (Card 12) Functional Block Diagram

When synchronization is attained, the $\overline{\text{Sync}}$ output is a ONE level which causes the FRAME SYNC indicator to extinguish.

The synchronization status level (Sync output at pin 33) also performs control functions on the decommutator card, servo DAC card, and servo control card. The channels per frame counter reset pulse is inverted and routed from pin 35 on card 12 to the decommutator card and the servo DAC card.

4.3.14 Servo Loop Circuits (Ref. Figure 4-19)

The functions of the servo loop circuits are to provide DC restoration (compensation for DC offset of the PAM input signal) before synchronization is attained and, after synchronization is achieved, to monitor specific channels of the input data format in order to generate correction signals used to establish precise full-scale and zero-scale data levels. The servo loop is composed of servo DAC printed-wiring board, card 4; servo adder printed-wiring board, card 5; and servo control printed-wiring board, card 6. Due to the interrelationship of these cards the servo loop circuits are described on an overall basis rather than at the individual card level.

All circuits of the DC restorer function are located on servo DAC card 4. These circuits consist of counter control circuit U11 through U14, a four-stage binary up/down counter U15, and a summing network. Before synchronization is obtained (sync input at pin J4-39 at ZERO level) and when not in the calibration mode of operation ($\overline{\text{CAL}}$ input at pin J4-16 an open) the counter control circuits monitor the overscale and underscale signal levels received from frame sync recognition card 10. (Refer to paragraph 4.3.12.) These signals control the direction of counting for the up/down counter. If the overscale signal is a logic ONE level, the counter clock pulses, gated 0° and 180° strobe pulses, causes the counter value to increase by one. If the underscale signal is a logic ONE the counter value is decreased by one with the clock pulse. With no offset error in the input signal the up/down counter will contain a mid-range count. Thus, each incremental increase or decrease from the mid-range count provides approximately 6.25 percent correction of the peak offset error. (DC offset may be as great as ±50% of peak-to-peak range of the input data.) The count contained in the up/down counter provides inputs to the summing network composed of resistors R22 through R25. The summing network produces discrete currents for each of the 16 possible counts of the up/down counter. These currents, produced by the DC restorer summing network, are then summed with the output of the zero-scale servo ladder network at the input to operational amplifier U19. The output from U19 is coupled through SERVO switch A2S3 to the input amplifier card 19 to compensate for DC offset. Since the overscale and underscale signals represent DC offset of 10 percent or greater, the DC restorer provides only a coarse adjustment of the offset error. Fine adjustment (within approximately 0.1 percent of the optimum level) is provided once synchronization is attained by correction of the minimum data level in the zero-scale servo loop which is described in subsequent paragraphs.

When the Model 515 advances to the lock mode (sync input at pin 22 of card 6 a ONE), the zero servo loop and the full-scale servo loop are activated at specific points of the input data format if certain conditions exist. The servo activate circuits (U5 and U15 through U18 on card 6) produce a zero data activate command, ZDA, when the channels-per-frame count corresponds to the channel

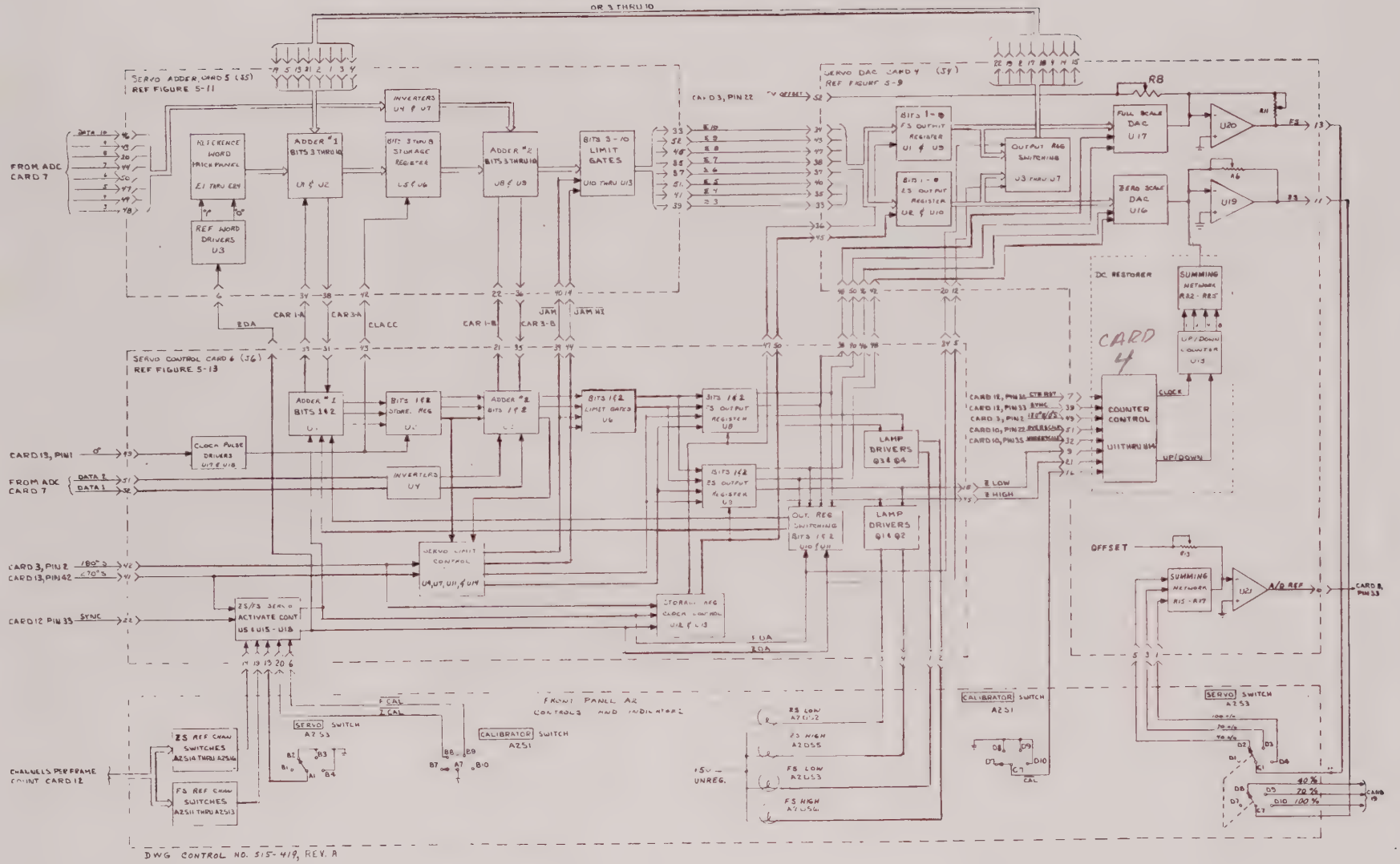


Figure 4-19. Servo Loop Functional Block Diagram

number programmed on the front panel ZERO REF CHAN switches A2S14 through A2S16. The servo activate control circuits produce a logic ONE FDA command (full-scale data activate) when the channels per frame count corresponds to the channel number programmed on the FS REF CHAN switches A2S11 through A2S13.

Generation of the FDA command signal is inhibited when CALIBRATOR switch A2S1 is in the 0% position and the ZDA command is inhibited if switch A2S1 is in the 100% position. Both the ZDA and FDA commands are inhibited if the CALIBRATOR switch A2S1 is in the 50% position or if the SERVO switch A2S3 is in the OFF position.

The functional operation of both the zero servo loop and the full-scale servo loop is the same. Both loops share the same processing and control circuits and have identical storage registers, digital-to-analog converter stages, and output amplifiers. In general, the zero servo loop provides fine correction for DC offset of the input signal by comparing the binary data output for a known data channel (zero reference channel) with an internally generated reference word. The difference is stored and converted to a DC level which provides a level shift in the input signal equal and opposite to the accumulated error. Similarly, the full-scale servo loop establishes the optimum maximum data level for the binary output of the Model 515 by comparing a known data channel (full-scale reference channel) with an internally generated reference word. The difference provides correction to the A/D reference level applied to the ladder and switches card thereby establishing the optimum maximum data level. Thus, by correcting the minimum data (zero-scale) and maximum data (full-scale) levels for known channels of the input format, the output data for all other channels is proportionally corrected. Since the operation of each servo loop is functionally the same, the following paragraphs discuss only the operation of the zero servo loop in detail.

When the servo activate control circuits generate a ZDA command the reference word patch area, E1 through E24 on card 5, produces the eight least significant bits of the 10-bit internal zero reference word. The two most significant bits of this reference word are developed at the bits 1 and 2 stages of adder #1 (U1 on card 6) from the logic ZERO FDA level. Thus, during the period of the zero reference channel in the input format, the internally generated reference word is 0001100010 which represents a binary value approximately nine percent greater than a 10-bit number of all ZEROS.

NOTE

During the period of the full-scale reference channel in the input format the ZDA and FDA command levels are complemented thereby complementing the internally generated reference word. The resultant reference word 1110011101 is approximately nine percent less than a binary word of all ONE bits.

The internally generated zero reference word is summed in adder #1 with the content of the zero-scale output register (U2 and U10 on card 4 and U9 on card 6).

This register contains the zero-scale correction data word developed from the previous cycle of the zero servo loop. The content of the zero-scale output register is gated to adder #1 via the output register switching gates (U3 through U8 on card 4 and U10 and U11 on card 6) which are enabled by the ZDA command. The sum produced by adder #1 is loaded into associated stages of the storage register composed of U5 and U6 on card 5 and U2 on card 6 by the 0° strobe pulse.

Functionally, adder #2 subtracts the binary value of the output data word representing the zero reference channel from the sum produced by adder #1. The 10-bit output data words received from the analog-to-digital conversion circuits are inverted by inverter stages U4 and U7 on card 5 and U4 on card 6. Thus, the output of adder #2 is the sum of the internally generated reference word plus the zero-scale correction word generated during the preceding cycle less the binary value of the zero reference channel output word. The outputs from adder #2 are coupled through limit gates (U10 through U13 on card 5 and U6 on card 6) and loaded into the zero-scale output register by the 180° strobe pulse generated during the period of the zero-scale channel. Thus, if the internally generated reference word and the output data word produced for the zero reference channel of the input format are equal, the content of the zero-scale output register generated during the preceding zero servo cycle is correct and remains the same for the next frame of input data. However, if the output data word is greater or less than the internally generated reference word, the correction word output from adder #2 changes by an amount equal and opposite to the magnitude of the detected error. The new zero-scale correction word is converted to a DC level by ladder network U16 and coupled through amplifier U19 and contacts of SERVO switch A2S3 to the input summing point on input amplifier card 19. The SERVO switch controls the rate of correction per frame for detected errors by controlling the gain of the zero correction loop. Correction rates of 40%, 70%, or 100% are selectable with the specific rate selected being based on the average quality of the input signal.

The 10-bit correction numbers produced by the zero-scale and full-scale servo loops provide 1024 incremental steps of fine correction for DC offset and the full-scale data level, respectively, after the initial DC offset correction has been accomplished by the DC restorer circuits. The resultant 512 incremental steps in each direction from a mid-range value provide a fine correction range of approximately ±20 percent of the full-scale value with a resolution of approximately ±0.02 percent of full scale. Thus, the maximum correction limits for each loop are all ZEROs for high level errors and all ONEs for low level errors. If a servo loop attempts to exceed the limits of the correction range, the content of the associated loop output register is locked at the applicable limit to prevent the servo from hunting. For example, assume the content of the zero-scale servo loop were all ZEROs. This condition indicates that the servo loop has just reached the limit of the correction range when compensating for a positive (with respect to data) offset. If the offset were to continue to increase, the zero loop would attempt to reduce the content of the output register causing the register value to recycle. However, this action is inhibited by the limit control circuits which clamp the correction number at all ZEROs and inhibit any further correction until the input offset is reduced to a value within the correction range. Front panel indicator lights provide indication whenever the zero-scale or full-scale servo loops reach either the high or low limits of their ranges.

The limit control function is accomplished by the limit control circuits on card 6 which monitor the eleventh summing stages of adder circuits #1 and #2. A logic ONE output from the eleventh stage of adder #2 indicates that a correction limit of the operating servo loop has been exceeded. The bit value for the eleventh stage of adder #1 indicates the limit that has been exceeded. A logic ONE level in the eleventh stage of adder #1 indicates that the all ZEROs limit (data high) has been exceeded and a logic ZERO level indicates that the all ONEs limit (data low) has been exceeded. The above conditions are monitored by the limit control circuits (U4, U7, U11, and U14 on card 6) which provide control inputs to the limit control gates. If the all ZEROs limit is exceeded, the limit control circuits produce a logic ZERO JAM signal and a logic ONE JAM HI signal. This results in correction value produced in the applicable servo loop output register being locked at all ZEROs. If the servo loop attempts to exceed the all ONEs limit both the JAM and JAM HI signals are logic ZERO levels which cause the content of the output register to be clamped at all ONEs.

The servo limit control circuits also provide inputs to the servo output registers indicating high or low limit conditions. The stored limit conditions provide input levels for lamp driver circuits Q1 through Q4 on card 6. A lamp driver driven by a logic ONE level provides a DC return for its associated front panel indicator thereby causing the indicator to light.

A high or low limit condition detected in the zero servo loop also provides a control input to the DC restorer circuits. The Z HIGH or Z LOW signal produced by the zero servo loop causes the up/down counter to be incremented by one count in the appropriate direction. This additional count allows the zero servo loop to be reset to a point within the correction range without reverting to the search mode of operation. The Z HIGH or Z LOW signals indicate the direction of counting to the up/down counter and the channel rate counter reset pulse provides the counter clock input.

4.3.15 Decommutator Card (Ref. Figure 4-20)

The primary function of the decommutator printed wiring board, card 3, is to extract a selected 10-bit channel from the data format and to convert the digital value for the channel to analog form. The analog output for the decommutated channel is displayed on the front panel DECOM meter, A2M3, and is made available at rear panel connector A3J5 for distribution to peripheral equipment. Card 3 also contains circuitry for inhibiting the 10-bit parallel output data when the Model 515 is not in synchronization and processing circuitry for channel rate and frame rate output pulses.

The parallel output gates (U2, U4, and U6) are enabled during normal operation by a logic ONE output from the output inhibit gates, U18. The parallel 10-bit channel inputs received from the ladder and switches card are thus inverted and routed to the output buffers, card 2. If synchronization is lost (Sync input from card 12 a logic ZERO) a logic ZERO is applied to each of the parallel output gates. The value of each output bit from the decommutator card is thereby clamped at a logic ONE which, in turn, provides a logic ZERO output for each bit output from card 2. The front panel CALIBRATOR switch, A2S1, provides

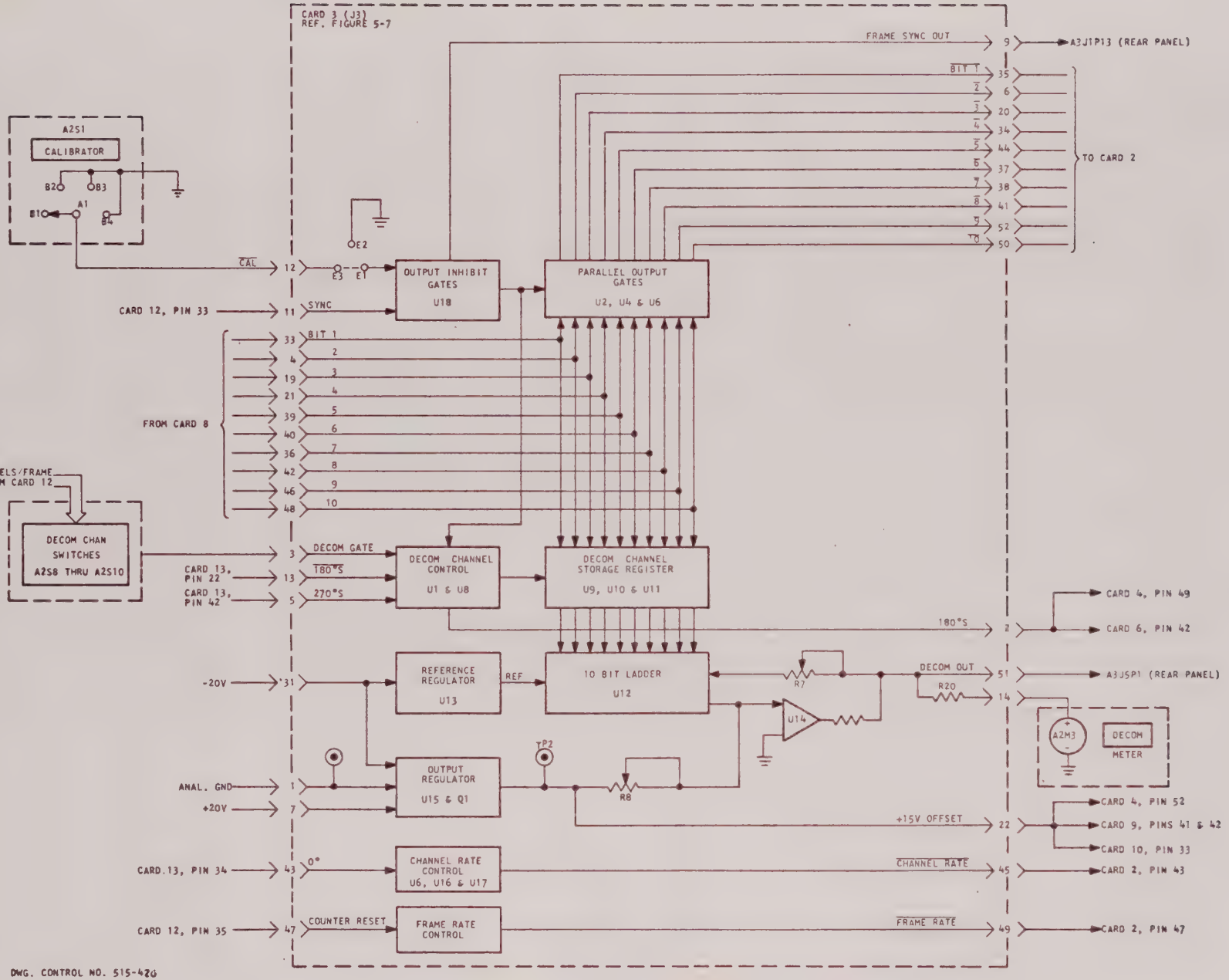


Figure 4-20, Decommutator (Card 3) Functional Block Diagram

a means of overriding the output inhibit function. When operating in the calibration mode, a ground level CAL input is applied to pin 12 and coupled through normally jumpered terminals E3 and E1 and the inhibit gates to provide a logic ONE enable input to the output gates regardless of the status of synchronization. The output inhibit gates also process the sync input at pin 11 which provides the frame Sync Out level at pin 9.

The 10-bit input received from card 8 at the channel rate are also applied to the decom channel storage flip-flops contained in U9, U10, and U11. When the channels-per-frame counter, card 12, is incremented to the number programmed on the front panel DECOM CHAN switches a logic ONE pulse is applied to pin 3. This gate input is AND'ed with the 270° strobe pulses produced by the clock generator to generate a negative-going set trigger for flip-flop U8. When U8 is in the set state, the next 180° strobe pulse applied to pin 13 is inverted and gated to the decom channel storage register causing the selected channel of data to be stored. The 180° strobe also clocks the flip-flop to the reset state thereby preventing the loading of another channel of data until the next decom gate pulse.

The stored 10-bit word is applied to 10-bit ladder circuit U12. This circuit converts the digital data to a representative analog value. The analog output is coupled through amplifier U14 to the front panel DECOM meter, A2M3, and to rear panel connector A3J5. Reference regulator furnishes a stable operating voltage input (−12V) for the digital-to-analog conversion function. The output regulator circuit, U15 and Q1, generates a +15 volt offset level which is used to regulate the voltage range of the analog output (nominally +5V to −5V). The +15 volt offset is also routed to the servo DAC, card 4, the sample and hold function, card 9, and frame sync recognition, card 10.

The channel rate control circuit, U6 and U16, produces the channel rate output pulse from the 0°clock (rectangular wave) signal received from the clock generator. The control circuit consists of two one-shot stages which produce a negative-going output pulse ($\overline{\text{Channel Rate}}$) for each negative transition (leading edge) of the clock input. The output pulse is approximately 500 nanoseconds in duration and is delayed approximately 2 microseconds from the leading edge of the clock input. This delay is provided to insure that the digitized data are stabilized before being used by external devices.

The frame rate control circuit is functionally the same as the channel rate control. This circuit produces a 500 nanosecond, negative-going pulse ($\overline{\text{Frame Rate}}$) delay approximately 4 microseconds with respect to the leading edge (positive transition) of the counter reset input pulse. Both the $\overline{\text{Channel Rate}}$ and $\overline{\text{Frame Rate}}$ signals are coupled to the output buffers, card 2.

4.3.16 Output Buffer Card (Ref. Figure 5-4)

The output buffer printed-wiring board, card 2, is composed of three SG-142 integrated circuit modules each of which contains four single input NAND-gates. These gates provide logic level inversion and output drive capability for the

10 discrete data bit levels, the channel rate pulse, and the frame rate pulse. All inputs to output buffer circuit are received from the decommutator circuit, card 3, and all outputs are routed to rear-panel connector A3J1. The frame rate output pulse is also routed to the front-panel FRAME RATE test jack A2TP2.

4.3.17 Primary AC and DC Power Circuits Description (Ref. Figure 4-21)

The primary AC power input, applied to the rear-panel power input connector A3P1, is coupled to one side of transformer A1T1 and through rear-panel fuse A3F1 to front-panel POWER switch A2S2. As the POWER switch is energized, primary power is connected across the primary windings of A1T1 and is applied to rear-panel fan A3B1. Secondary windings of A1T1 are connected across full-wave diode-bridge rectifier circuits A1CR1, A1CR2, and A1CR3. These rectifiers supply unregulated DC voltages to the regulator circuits on the Regulator Card, Card 21.

Five primary regulator circuits and two secondary regulators are included on the Regulator Card. The five primary regulators are integrated-circuit/transistor regulator circuits. Each of the five primary regulators contains an output voltage adjustment potentiometer. Secondary regulators (+12-volt and −6-volt) consist of zener diodes which are connected across the +15-volt and −15-volt regulated outputs.

The +5-volt regulator contains a power transistor located external to the card. This transistor provides a high-current output from the +5-volt regulator required because of the high loading characteristics of the +5 volts.

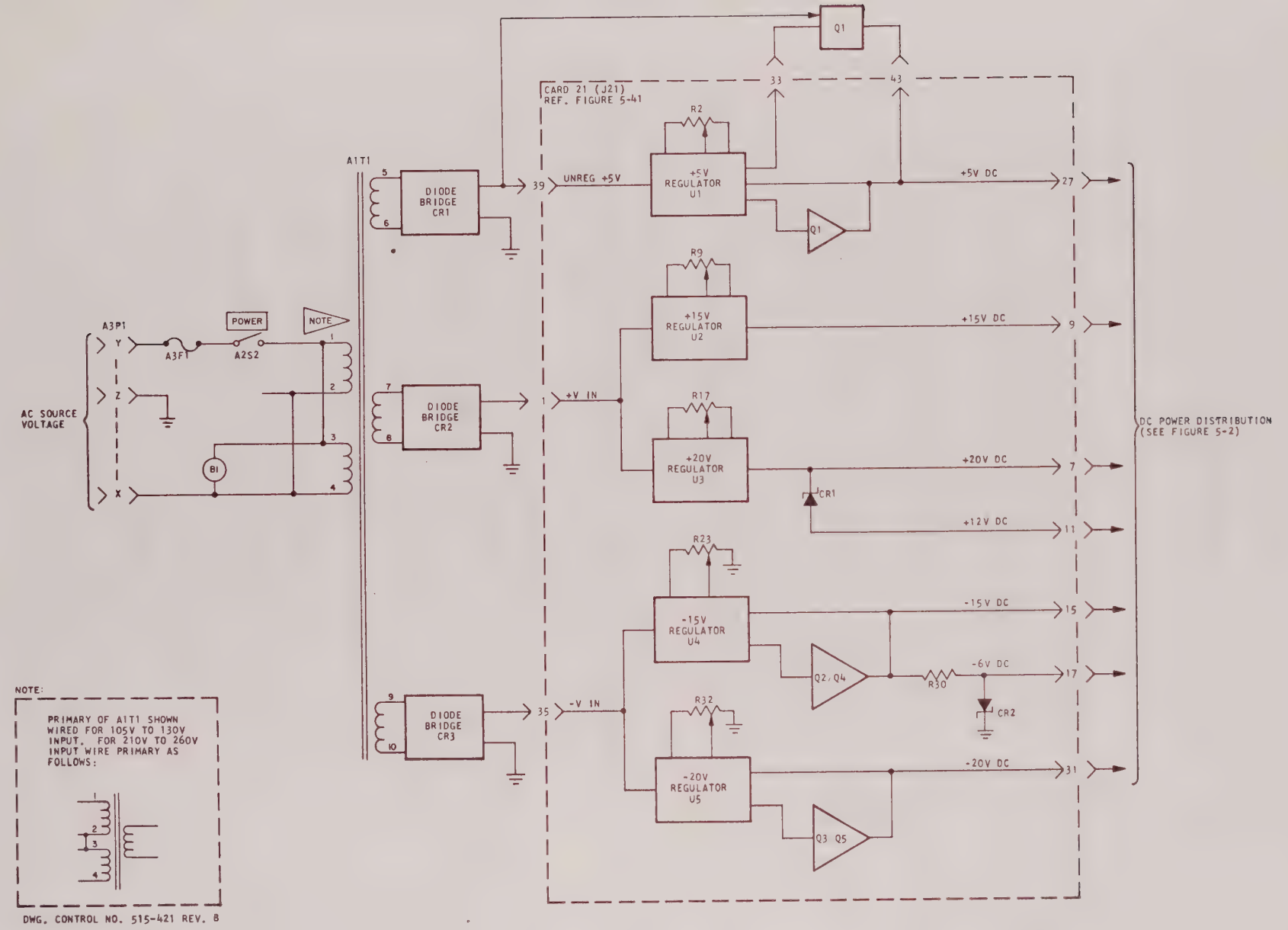


Figure 4-21. Power Supply and Voltage Regulator (Card 21) Functional Block Diagram

SECTION 5

MAINTENANCE

5.1 GENERAL

This section provides information intended to aid maintenance personnel in evaluating the operational status of the Model 515 PAM/PDM Synchronizer and for restoring the unit to an optimum condition in the event of a malfunction. Evaluation of the operational status is based on the results of the checkout procedures outlined in paragraph 5.2. The individual checkout procedures are referenced to functional circuits of the 515 and therefore, provide the first step in fault isolation if abnormal checkout indications which cannot be corrected by adjustment are obtained. Detailed fault isolation should be based on a thorough knowledge of normal circuit operation as provided in Section 4. In addition, complete assembly and schematic diagrams for the Model 515 are provided in Figures 5-1 through 5-42. Wire lists for the front and rear panels are provided in Tables 5-1 and 5-2, respectively.

5.2 CHECKOUT AND ADJUSTMENT PROCEDURES

5.2.1 Equipment Required

The following test equipment, or equivalents, are requirements for performing the checkout and adjustment procedures:

a. PAM Simulator -- EMR Model 517

b. Oscilloscope -- Tektronix Model 545 with Type 82 Dual Trace Plug-In Unit

c. Digital Voltmeter -- Hewlett-Packard Model 3460A

d. Oscillator -- Hewlett-Packard 200CD

e. VTVM -- Hewlett-Packard 400D

f. Frequency Meter -- Berkley/Beckman EPUT Meter

g. Millivolt Standard -- EDC Model MV 100N

CAUTION

Always turn off power when inserting or removing printed-wiring boards or jumpers.

5.2.2 Power Checks and Adjustments

a. Turn off power and install regulator card 21 on the card extender.

b. Turn power on.

c. Connect the digital voltmeter to J21-9 and adjust potentiometer R5 for an indication of +15 ±0.05 volts.

d. Connect the digital voltmeter to J21-7 and adjust potentiometer R1 for an indication of +20 ±0.05 volts.

e. Using the digital voltmeter monitor for +12 ±1.0 volts at J21-11. (Not adjustable)

f. Connect the digital voltmeter to J21-27 and adjust potentiometer R37 for an indication of +5 ±0.02 volts.

g. Connect the digital voltmeter to J21-15 and adjust potentiometer R38 for an indication of −15 ±0.05 volts.

h. Connect the digital voltmeter to J21-31 and adjust potentiometer R41 for an indication of −20 ±0.05 volts.

i. Connect the digital voltmeter to J21-17 and observe indication of −6.2 ±0.6 volts. (Not adjustable)

5.2.3 Input Amplifier Checks

Check the operation of the input amplifier card as follows:

a. Set the front panel CALIBRATOR switch A2S1 and SERVO switch A2S3 to the OFF position.

b. Apply a zero volt signal to rear panel connector A3J4.

c. Using a VTVM observe the voltage level at the front panel INPUT test jack. The voltage level should be +5 ±0.5 volts.

d. Connect the test oscillator to connector A3J4 and adjust for a 1 volt ±0.1 volt peak-to-peak signal at a frequency greater than 100 kHz.

e. Observe that the front panel INPUT meter will read in the green area by adjusting the INPUT potentiometer

A2R1. Perform this step with CODE switch A2S7 in both the RZ and NRZ positions and with POL switch A2S4 in both the NORM and INV positions.

f. Increase the amplitude of the test oscillator signal to 5 ±1 volts peak-to-peak.

g. Connect an oscilloscope to the INPUT test jack and adjust the INPUT potentiometer until the waveform limits at both peaks. The limiting levels should be −1.5 ±1.0 volts and +9 ±1.0 volts.

5.2.4 Input Filter Checks

Check the operation of the input filter card as follows:

a. Apply a zero volt signal to rear panel connector A3J4.

b. Adjust potentiometer R36 on card 19 until the filter output (pin 4) is within ±0.005 volts of the filter input voltage level (pin 1).

c. Connect the test oscillator to connector A3J4.

d. Set FILTER switch A2S6 to the IN position.

e. Using the Hewlett-Packard 400 D VTVM to monitor the filter input and output levels, adjust the INPUT potentiometer to maintain a 0 db reading on the meter when monitoring the filter input for each of the test frequencies required in step (f).

f. Set the front panel CHANNEL RATE switches as indicated below and observe the filter output for each of the two test frequencies associated with each setting:

CHANNEL RATE Switches	Test Frequency A (−3.0 db ±1.0 db max.)	Test Frequency B (−34 db ±5.0 db min.)
10.0 CH/S	10.0 Hz	50.0 Hz
100 CH/S	100 Hz	500 Hz
1.10 KCH/S	1.10 kHz	5.50 kHz
2.20 KCH/S	2.20 kHz	11.0 kHz
4.40 KCH/S	4.40 kHz	22.0 kHz
8.80 KCH/S	8.80 kHz	44.0 kHz
9.90 KCH/S	9.90 kHz	49.5 kHz
10.0 KCH/S	10.0 kHz	50.0 kHz
100 KCH/S	100 kHz	500 kHz

5.2.5 PDM-to-PAM Conversion Checks and Adjustments

To check the operation of PDM/PAM converter card, proceed as follows:

a. Connect Model 517 PAM/PDM Simulator to rear panel connector A3J4.

b. Program simulator for PDM output as follows:

1. Channel Rate -- 1 kHz.
2. Frame Length -- 30 CH/F.
3. Zero Reference -- Channel 1 (adjust pulse duration to desired percent of channel period).
4. Full Scale Reference -- Channel 2 (adjust pulse duration to desired percent of channel period).
5. Frame Sync Pattern -- Full amplitude pulse, the duration of which is 1.5T in a time interval of 2T. (T = one channel period.)
6. Signal Amplitude -- 4 volts peak-to-peak.
7. Polarity -- Normal.
8. DC Offset -- Zero (pulse centered about zero volts).

c. Set up 515 as follows:

1. Channel Rate -- 1 kHz.
2. Frame Length -- 30 CH/F.
3. Zero Reference -- Channel 1.
4. Full Scale Reference -- Channel 2.
5. Mode -- PDM.
6. Code -- NRZ.
7. Filter -- Out.
8. Polarity -- Normal.
9. Track -- Wide.
10. Frame Sync Pattern -- X F F F O

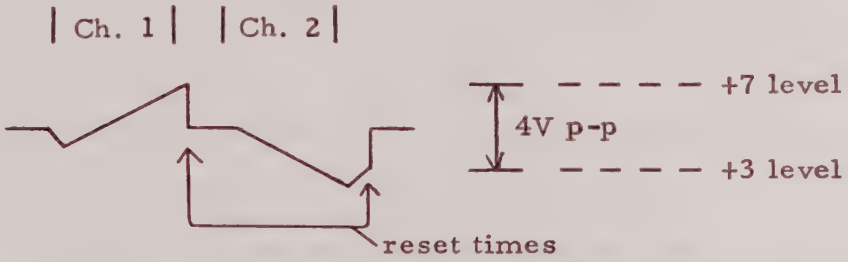
11. Cal -- Off.

12. Servo -- Off.

d. On Model 515, adjust INPUT potentiometer until INPUT meter reads in center of green area.

e. Observe channels 1 and 2 ramps at TP1 of PDM/PAM card with scope.

Adjust R19 on PDM/PAM card until the peak-to-peak difference between channel 1 and channel 2 at reset time is 4 volts.



f. To perform coarse offset adjust, adjust R23 until channel 1 peak is at +7 level.

g. To perform fine offset adjust, adjust R23 for a minimum shift of the waveform when the servo is switched between off position and 40%.

h. Place servo switch in 40% position.

i. Observe that the frame sync, channel sync and servo lights are off.

j. Shift the DC level of the incoming signal ± 50% and observe that the 515 maintains lock and all lights are off.

k. Return DC offset to zero.

5.2.6 Phase Locked Loop Checks and Adjustments

To check the circuits of the phase locked loop (clock generator card 13, VCO card 14, loop filter card 15, monostable card 16, and differentiator card 17) proceed as follows:

a. Connect the PAM simulator to rear panel connector A3J4 and program as follows:

1.	Channel Rate	- 10 KCH/S
2.	Frame Length	- 64 CH/F
3.	Code	- NRZ
4.	Polarity	- Normal
5.	Frame Sync Pattern	- O-F-F-F-1/2
6.	A Common	- 0%
7.	B Common	- 100%
8.	DC Offset	- None
9.	Signal Amplitude	- 1V peak-to-peak

10. Place a unique channel somewhere within the frame and adjust the voltage level until it represents a 20% transition from the adjacent channels.

b. Program the Model 515 to receive the test signal and adjust the front panel INPUT potentiometer until the INPUT meter reads in the center of the green band.

c. Connect the oscilloscope to test jack TP3 on differentiator card 17 and adjust potentiometer R14 on card 17 so that a narrow positive pulse occurs during the positive 20% transition.

d. Adjust potentiometer R17 on card 17 so that a narrow positive pulse occurs during the negative 20% transition.

e. Alternately adjust R14 and R17 until the unique channel is bracketed by the two pulses.

f. Connect the oscilloscope to test jack TP1 on monostable card 16 and adjust potentiometer R6 on card 16 to obtain a waveform with a duty cycle of 50% ±5%.

g. Remove the input signal from the Model 515.

h. Set the front panel TRACK switch to the NAR position and adjust potentiometer R55 on loop filter card 15 until the DEV meter reads zero.

i. Reconnect the input signal from the simulator to the Model 515.

j. Using a frequency meter, measure the simulator output frequency and adjust the frequency vernier on the simulator until an indication of 10 KCH/S ±10 CH/S is obtained.

k. Adjust potentiometer R6 on VCO card 14 until the front panel DEV meter indicates zero.

l. Program the simulator for no transitions during data channels by placing the A and B common channels at the same voltage level and removing the unique channels from the frame. The resultant waveform should be 64 CH/F with transitions only during the frame sync pattern.

m. To insure that the 515 is synchronized with the signal, observe the 0° clock at TP2 on clock generator card 13 while triggering the scope with the frame sync pulse from the simulator. The scope display should be synchronized.

n. Adjust R38 on differentiator card 17 while observing the CHAN SYNC light. Find the threshold (setting at which the light just turns off), then add an additional turn in a direction such that the light is off. Remove the signal and observe that the light turns on after a delay of approximately one second.

o. Restore the input signal.

p. On the simulator set A common for 0%, B common for 100%, and adjust the simulator frequency vernier until the deviation meter reads zero. Observe the input frequency.

q. With the TRACK switch in NAR position, vary the incoming frequency ±1%. Observe that the DEV meter reads on the edge of the red area when the input frequency is at ±1%.

r. Adjust the input frequency beyond ±1% and observe that the 515 drops out of sync.

s. Set the TRACK switch to WIDE position and the CHANNEL RATE switches to 11.0 KCH/S. Observe

that the 515 remains in sync when the channel rate switches on the simulator are set to 10.0 KCH/S and 12.0 KCH/S.

t. Observe the following signals on clock generator card 13 with a scope:

Pin 34 - 0° clock
Pin 41 - 90° clock
Pin 21 - 180° clock
Pin 2 - 270° clock
} rectangular waveforms at channel rate

Pin 1 - 0° strobe -- positive pulse 150 ±50 nanoseconds
Pin 22 - 180° strobe -- negative pulse 60 ±20 nanoseconds
Pin 42 - 270° strobe -- positive pulse 60 ±20 nanoseconds

5.2.7 Synchronization Checks and Adjustments

a. Monitor TP2 on decommutator card 3 with a digital voltmeter and adjust R6 on card 3 for +15V ±0.01V.

b. Monitor pin 6 of servo DAC card 4 with a digital voltmeter. With the SERVO switch in the OFF position, adjust R13 on card 4 for +10V ±0.010V.

c. Observe the following signals at the 515 output connector A3J1:

Frame Rate Pulse (Pin A3J1-11) - a positive pulse approximately 600 nanoseconds wide occurring 4 µsec after negative transition of 0° clock.

Channel Rate Pulse (Pin A3J1-12) - a positive pulse approximately 600 nanoseconds wide occurring 2 µsec after negative transition of 0° clock.

d. Program the PAM Simulator as follows:

1.	Channel Rate	- 10 KCH/S
2.	Frame Length	- 64 CH/F
3.	Code	- NRZ
4.	Polarity	- Normal
5.	Frame Sync Pattern	- O-F-F-F-1/2
6.	A Common	- 0%
7.	B Common	- 100%
8.	DC Offset	- Zero
9.	Signal Amplitude	- 1V peak-to-peak

e. Connect the simulator test signal to A3J4 on the rear panel of the Model 515 and program the 515 to accept the test input.

f. Synchronize the 515 by increasing the INPUT control until the INPUT meter reads in the center of the green area. The FRAME SYNC and CHAN SYNC lamps should be off.

g. Perform the same test at the following channel rates: 10 CH/S, 100 CH/S, 1.11 KCH/S, 2.22 KCH/S, 4.44 KCH/S, 8.88 KCH/S, 100 KCH/S.

h. Return the channel rate to 10 KCH/S.

i. With the 515 synchronized, change the setting of each channel in the frame sync pattern on the 515 and observe that the FRAME SYNC lamp turns on when the channel is set to a position other than the correct pattern or an 'X' position.

j. Set the FRAME SYNC PATTERN switches on the simulator and the 515 to the following positions and observe that the frame sync lamp is off.

F O O O F

$\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$

O F F F O

k. Return the pattern to O-F-F-F-1/2.

l. Observe the underscale and overscale signals (pins 35 and 22, respectively, on frame sync card 10) with a scope. Both signals should be at logic ZERO.

m. Offset the input signal in a positive direction and observe that the overscale signal changes to a logic ONE.

n. Offset the input signal in a negative direction and observe that the underscale signal changes to a logic ONE.

o. Return the DC offset to zero.

5.2.8 Sample and Hold Card Checks

a. Connect an oscilloscope to pin 37 on sample and hold card 9. The observed sample pulse should return to

a logic ZERO level at 180° of the clock generator timing and remain in this state for approximately 5 microseconds.

b. Connect the oscilloscope to test jack TP1 on card 9 and adjust the output and offset controls on the simulator until the observed waveform swings between +7.5 ±0.4 volts and +2.5 ±0.4 volts.

c. Connect the oscilloscope to test jack TP2 on card 9. The observed waveform should swing between 0 ±0.4 volts and −10 ±0.4 volts.

5.2.9 Analog-to-Digital Conversion Checks

To check the operation of the A/D converter (ladder and switches card 8 and A/D timing card 9) proceed as follows:

a. Program the PAM Simulator as follows:

1.	Channel Rate	- 10 KCH/S
2.	Frame Length	- 64 CH/F
3.	Code	- NRZ
4.	Polarity	- Normal
5.	Frame Sync Pattern	- O-F-F-F-1/2
6.	A Common	- 0%
7.	B Common	- 100%
8.	DC Offset	- Zero
9.	Signal Amplitude	- 4 volts peak-to-peak

b. Connect the simulator test signal to input connector A3J4 on the Model 515 and synchronize the 515 to the simulator.

c. Set the front panel SERVO switch to OFF and set the FILTER switch to OUT.

d. Apply a stable external voltage (millivolt standard) to one of the unique channels and monitor this voltage with a digital voltmeter.

e. Set the DECOM CHAN switches on the 515 to the address of the unique channel in the simulator output containing the millivolt standard data.

f. Sync an oscilloscope on the channel decom pulse available at pin 3 of card 3.

g. Set the millivolt standard reference voltage to 0 ±0.001 volts and adjust the simulator offset until a binary count of 0000000000 is obtained at rear panel connector A3J1.

NOTE

See Table 5-1 for bit position/ pin number association.

h. Set the reference voltage to −5.000V ±0.001V and adjust the simulator gain until a binary count of 1111111111 is obtained.

i. Alternate between steps (g) and (h) until both conditions are satisfied.

j. Adjust the reference to the following voltages and observe that the binary count is within the given tolerances:

Reference	Binary Count
−0.621V ±0.005V	0001111111 ±3 counts
−1.246V ±0.005V	0011111111 ±3 counts
−2.498V ±0.005V	0111111111 ±3 counts
−2.503V ±0.005V	1000000000 ±3 counts
−3.754V ±0.005V	1100000000 ±3 counts
−4.370V ±0.005V	1110000000 ±3 counts

k. Set the reference voltage to −2.503 ±0.005 volts.

l. Connect a digital voltmeter to the decom channel output connector A3J5 and adjust potentiometer R8 on card 3 to obtain a reading of +0.005 ±0.01 volts.

m. Set the millivolt standard reference voltage level at −5.000 ±0.001 volts and adjust potentiometer R7 on card 3 to obtain a reading of +5 ±0.010 volts.

n. Leave equipment set up for checks of paragraph 5.2.10.

5.2.10 Servo and DC Restorer Checks and Adjustments

To check the operation of the servo loop (servo DAC card 4, servo adder card 5, and servo control card 6) proceed as follows:

a. Verify that the simulator and Model 515 are still programmed as outlined in step (a) of paragraph 5.2.9.

b. Program the ZERO REF CHAN switches for 060 and the FS REF CHAN switches for 062 (first and third channels, respectively, of the frame sync pattern).

c. Set the SERVO switch to OFF.

d. Jumper pin 13 of servo control card 6 and pin 2 of microcircuit U3 on card 6 to ground.

e. Connect an oscilloscope to pin 13 of servo DAC card 4 and adjust potentiometer R11 to obtain a 10 ±0.4 volt peak-to-peak amplitude for the observed sawtooth waveform. Adjust potentiometer R8 on card 4 to center the waveform about 0 volt.

f. Connect the oscilloscope to pin 11 of card 6 and adjust potentiometer R6 to obtain a 4 ±0.2 volt peak-to-peak amplitude for the observed sawtooth waveform.

g. Remove the jumpers from the servo control card.

h. While varying the INPUT control over the range of the green area on the INPUT meter observe that the voltage display on the digital voltmeter remains constant. (See step (m) of paragraph 5.2.8.)

i. Repeat step (h) with the SERVO switch in the 40%, 70%, and 100% positions.

j. Reset the INPUT control to the point at which the INPUT meter reads in the center of the green area.

k. Vary the input signal DC level ±50% with the simulator offset control and observe that the 515 maintains channel and frame sync.

l. Return the DC offset to zero volt.

5.3 IC REFERENCE DIAGRAM

Figures 5-43 through 5-51 illustrate the schematic or logic configurations for individual integrated circuit modules not shown functionally on the Model 515 logic diagram. The IC diagrams are for reference only since individual modules are nonrepairable.

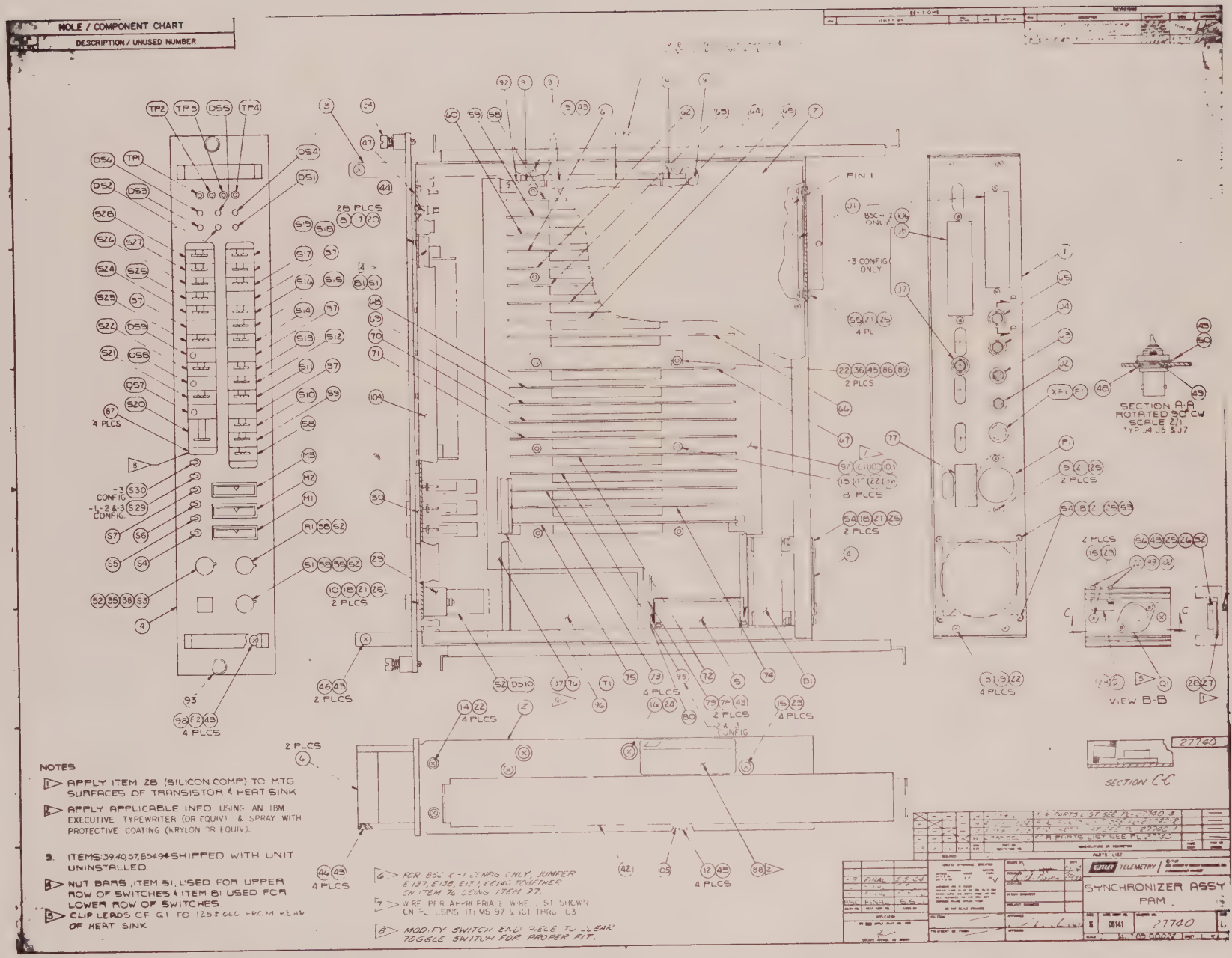
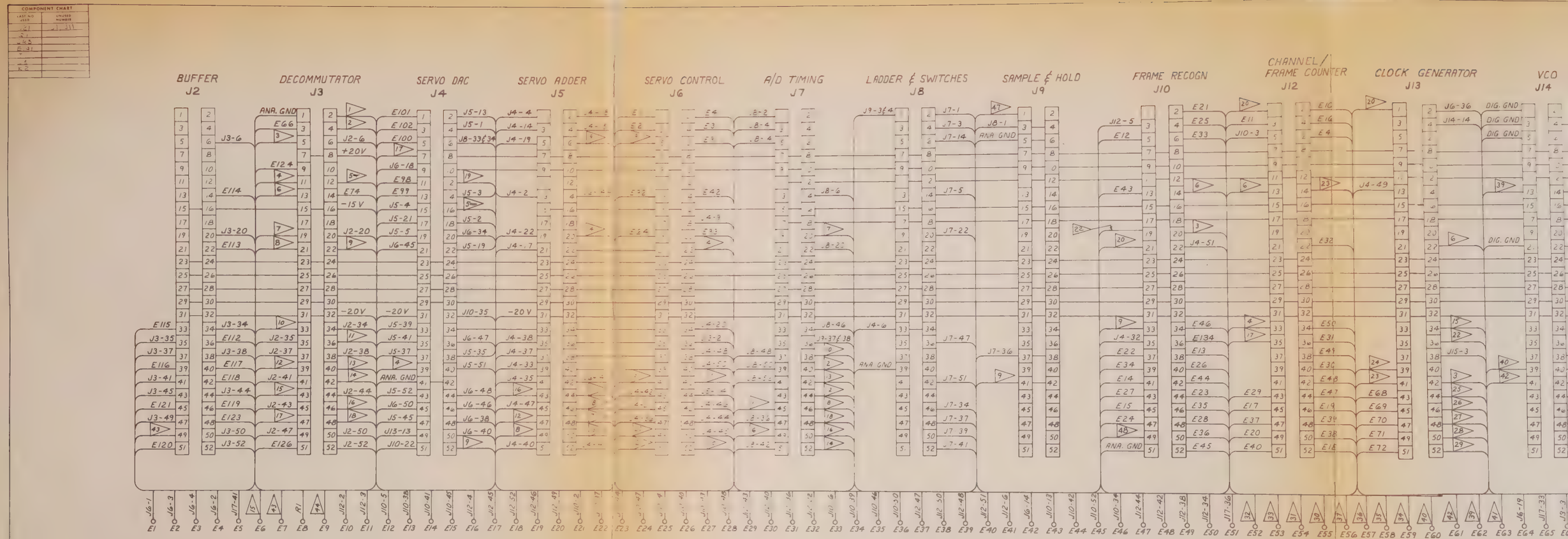


Figure 5-1. Model 515 PAM/PDM Synchronizer Assembly Diagram



NOTES:

1. J3-2, J6-42
2. J3-4, J6-51, J7-40
3. J3-5, J6-41, J10-20, J13-42, J18-13
4. J3-11, J4-39, J6-22, J12-33
5. J3-12, J4-16, E82, J18-34
6. J3-13, J7-49, J10-14, J12-13, J13-22, J18-14
7. J3-19, J5-48, J7-20
8. J3-21, J5-49, J7-46
9. J3-22, J4-52, J9-4, E42, J10-33
10. J3-33, J6-52, J7-38
11. J3-36, J5-44, J7-45
12. J3-39, J5-47, J7-44
13. J3-40, J5-50, J7-42
14. J3-42, J5-20, J7-52
15. J3-43, J13-34, J17-37, E6
16. J3-46, J5-43, J7-50
17. J3-47, J4-7, J12-35
18. J3-48, J5-46, J7-48
19. J4-12, J5-6, J6-5
20. J6-49, J10-21, J12-1, J13-1
21. J19-4, J18-1, E137
22. E135, J13-36, J17-14, E77, J10-19
23. J12-14, J13-41, J17-22
24. J18-39, J17-2, E78
25. J13-44, J15-43, J16-43, J17-43, J19-43
26. J13-46, J15-45, J16-45, J17-45, J19-45
27. J13-48, J15-47, J16-47, J17-47, J18-47, J19-47
28. J13-50, J15-49, J16-49, J17-49, J18-49, J19-49
29. J13-52, J15-51, J16-51, J17-51, J18-51, J19-51
30. J14-38, J16-38, J17-38, J18-38, E55, J15-38, J19-38
31. J14-40, J15-40, J16-40, J17-40, J18-40, E54, J19-40
32. J14-42, J15-42, J16-42, J17-42, J18-42, E52, J19-42
33. J14-44, J15-44, J16-44, J17-44, J18-44, E53, J9-44
34. J14-46, J15-46, J16-46, J17-46, J18-46, E59, J9-46
35. J14-48, J15-48, J16-48, J17-48, J18-48, E58, J9-48
36. J14-50, J15-50, J16-50, J17-50, J18-50, E57, J9-50
37. J14-52, J15-52, J16-52, J17-52, J18-52, E56, J9-52
38. J15-2, J16-4, J17-39
39. J14-3, J16-1, E62
40. J14-39, J16-2, E60
41. J14-4, J16-3, E63
42. [illegible]
43. J2-49, J22, E7
44. E9, CR1, C1, (E110-5 UNREG)
45. Q1 NOT LOCATED ON INTERCONNECT BOARD. ALSO AIR
46. T1 NOT LOCATED ON INTERCONNECT BOARD
47. J18-4, J9-1, E38
48. J18-33, J9-49, E39
49. J18-35, J7-35, E140
50. WHEN PDM/PAM CONVERTER BOARD (J18) IS NOT USED. E137, E138, E139 AND E140 ARE JUMPERED TOGETHER.

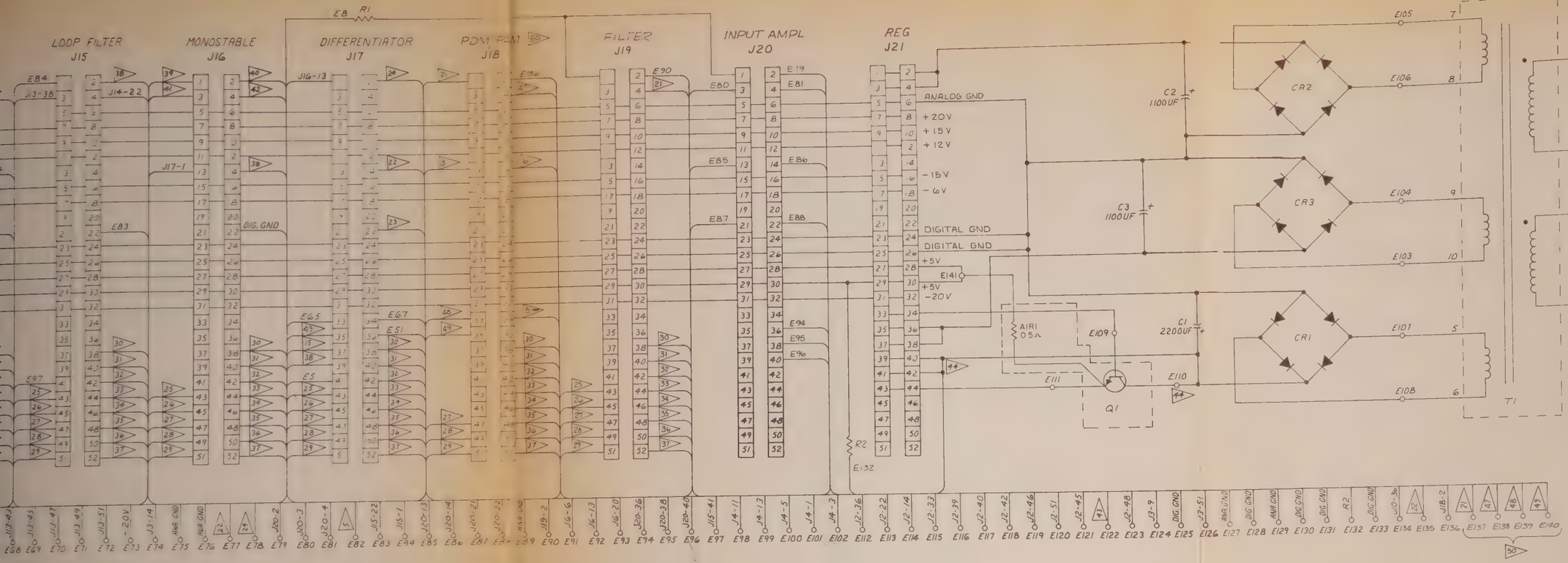


FIGURE 5-2. MODEL 515-03
INTERCONNECTION BOARD AI
WIRING DIAGRAM

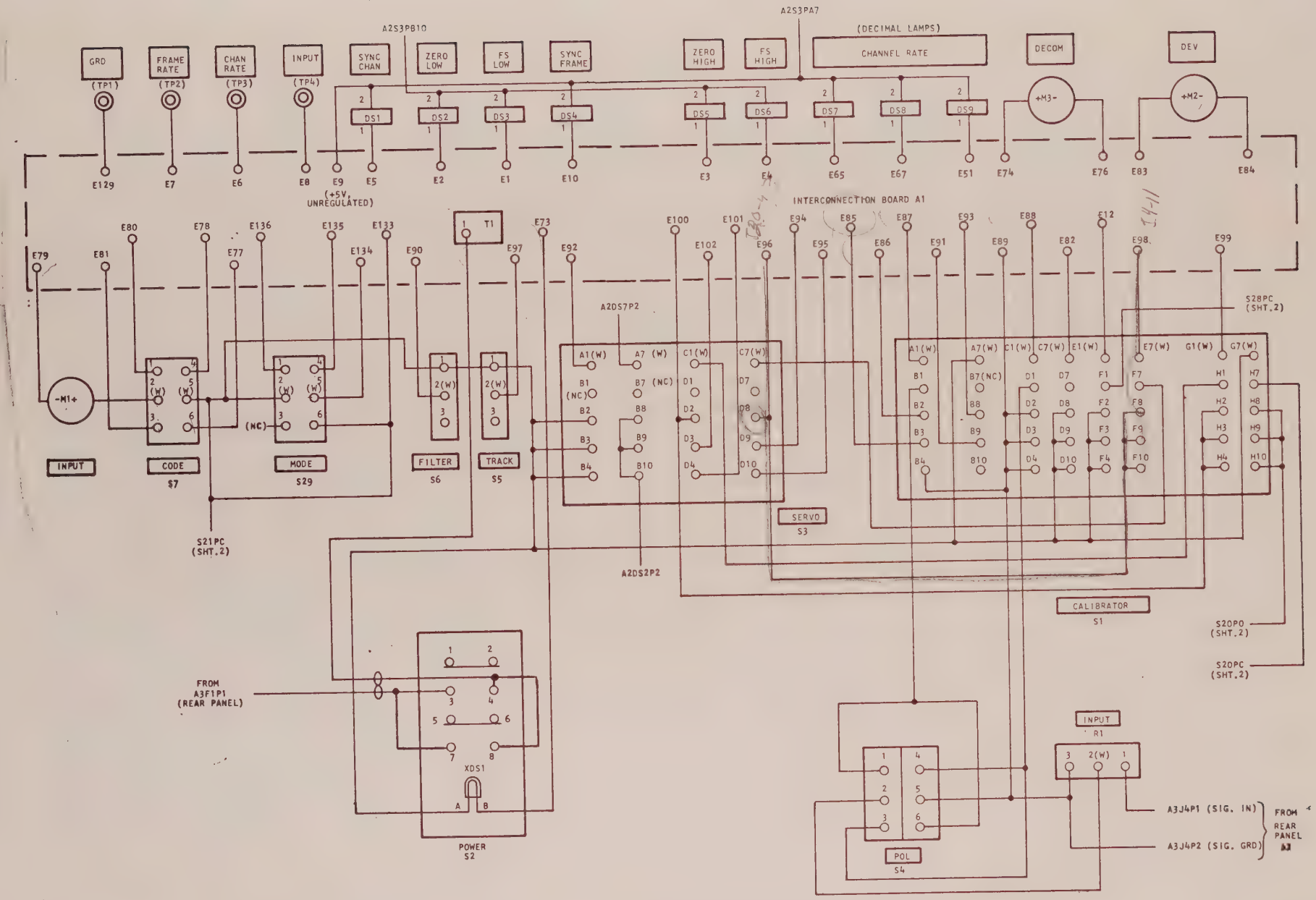


Figure 5-2A (Sheet 1 of 2). Model 515-03 Front Panel A2 Wiring Diagram

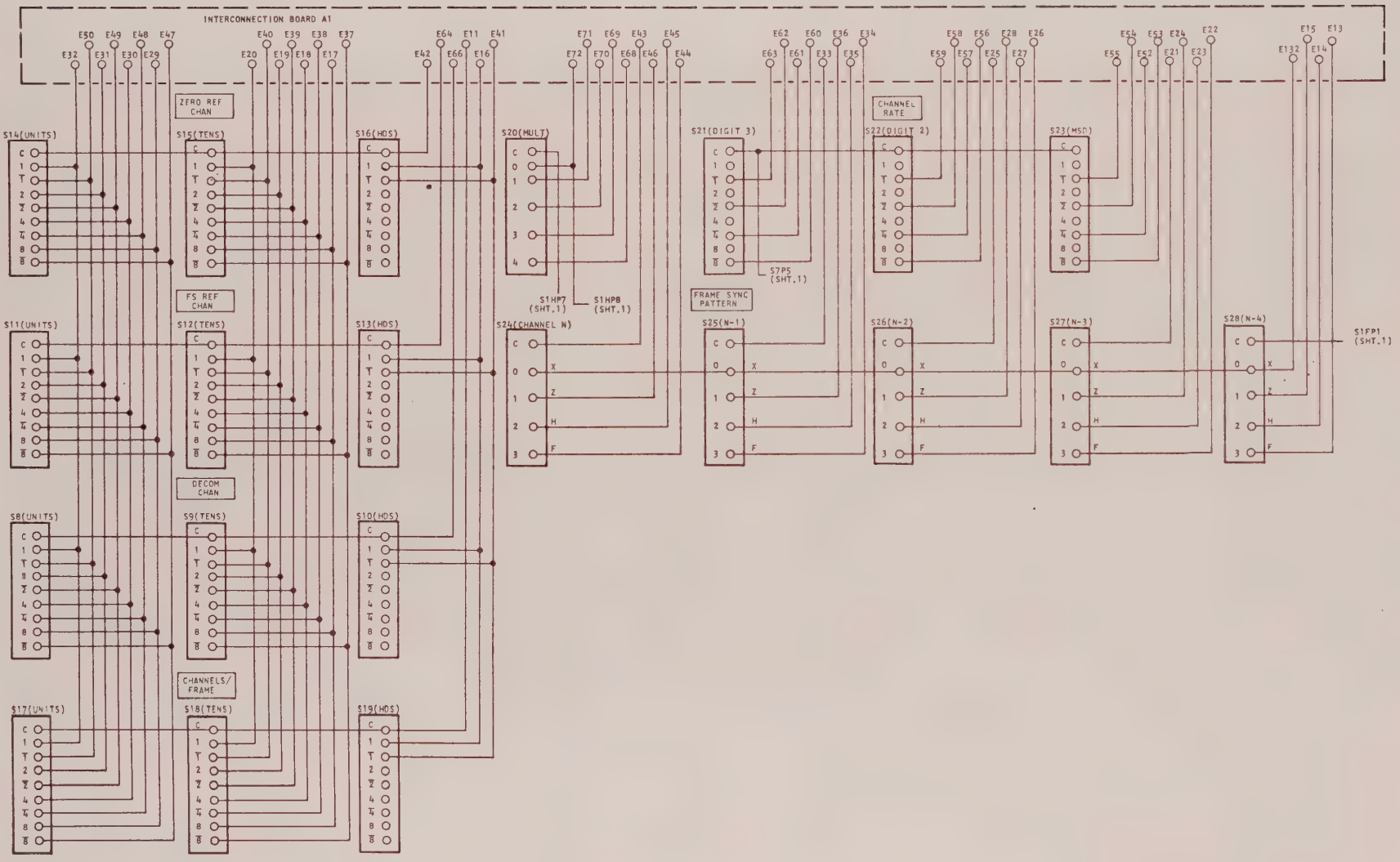


Figure 5-2A (Sheet 2 of 2). Model 515-03 Front Panel A2 Wiring Diagram

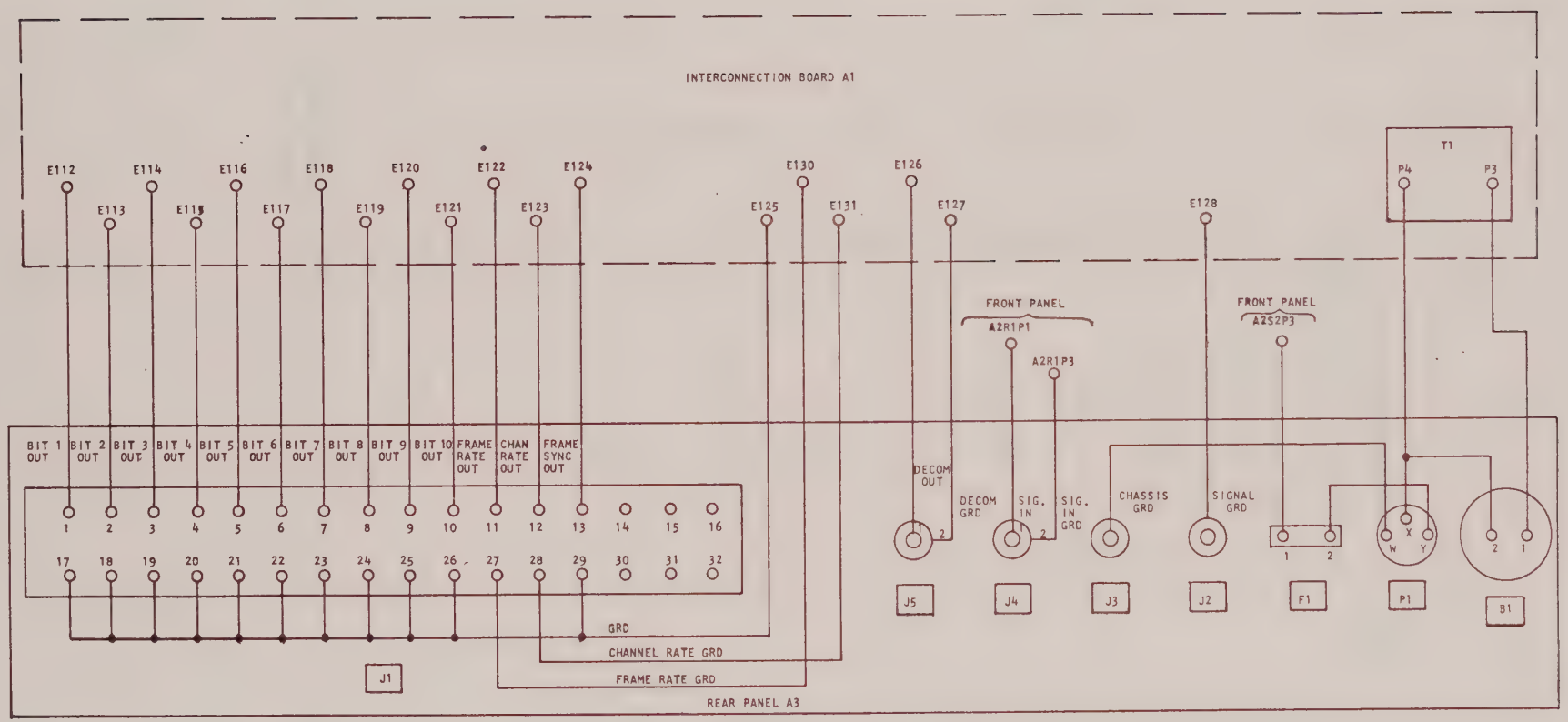


Figure 5-2B. Model 515-03 Rear Panel A3 Wiring Diagram

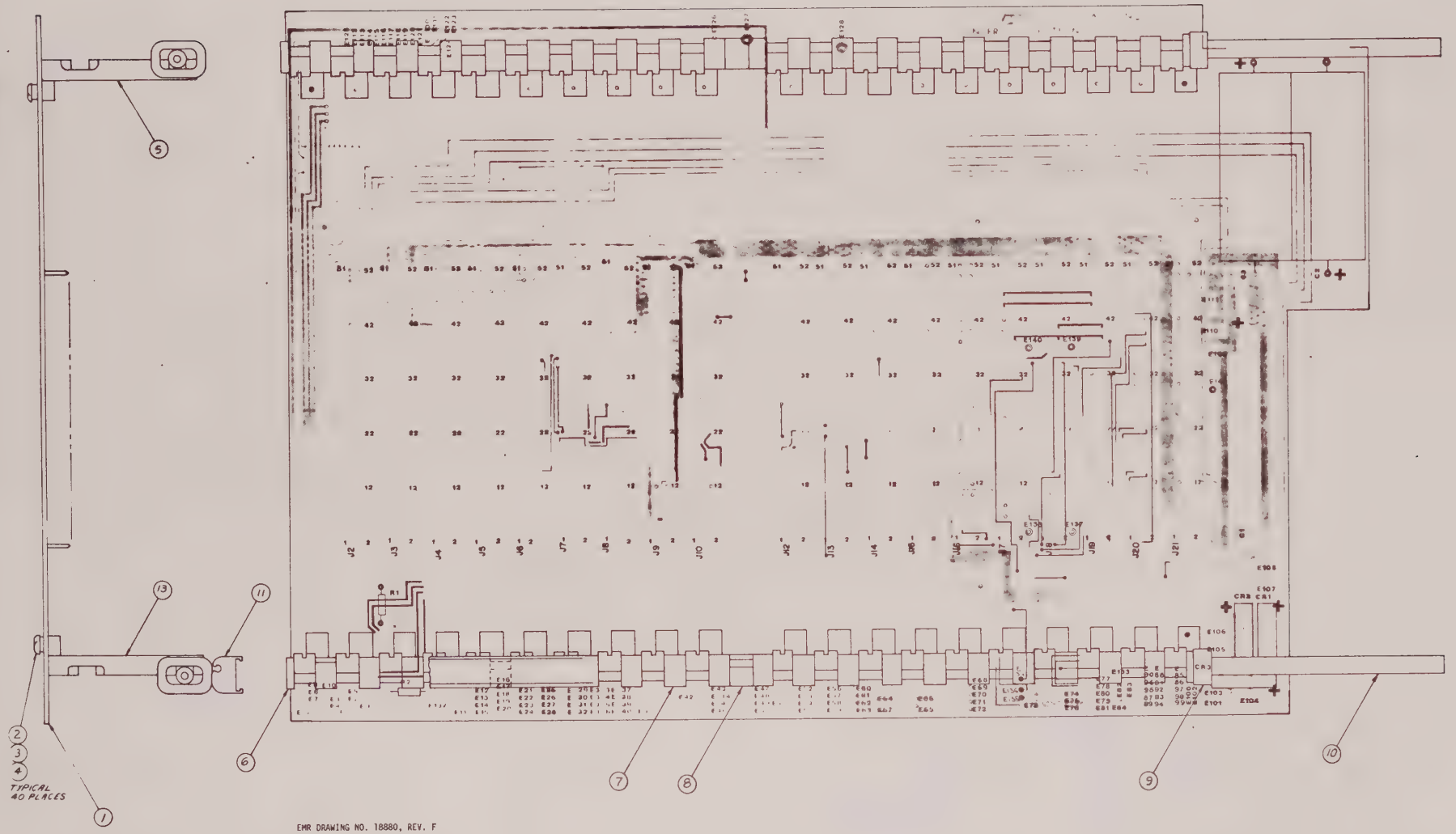


Figure 5-3. Interconnection Printed-Wiring Board Assembly Diagram

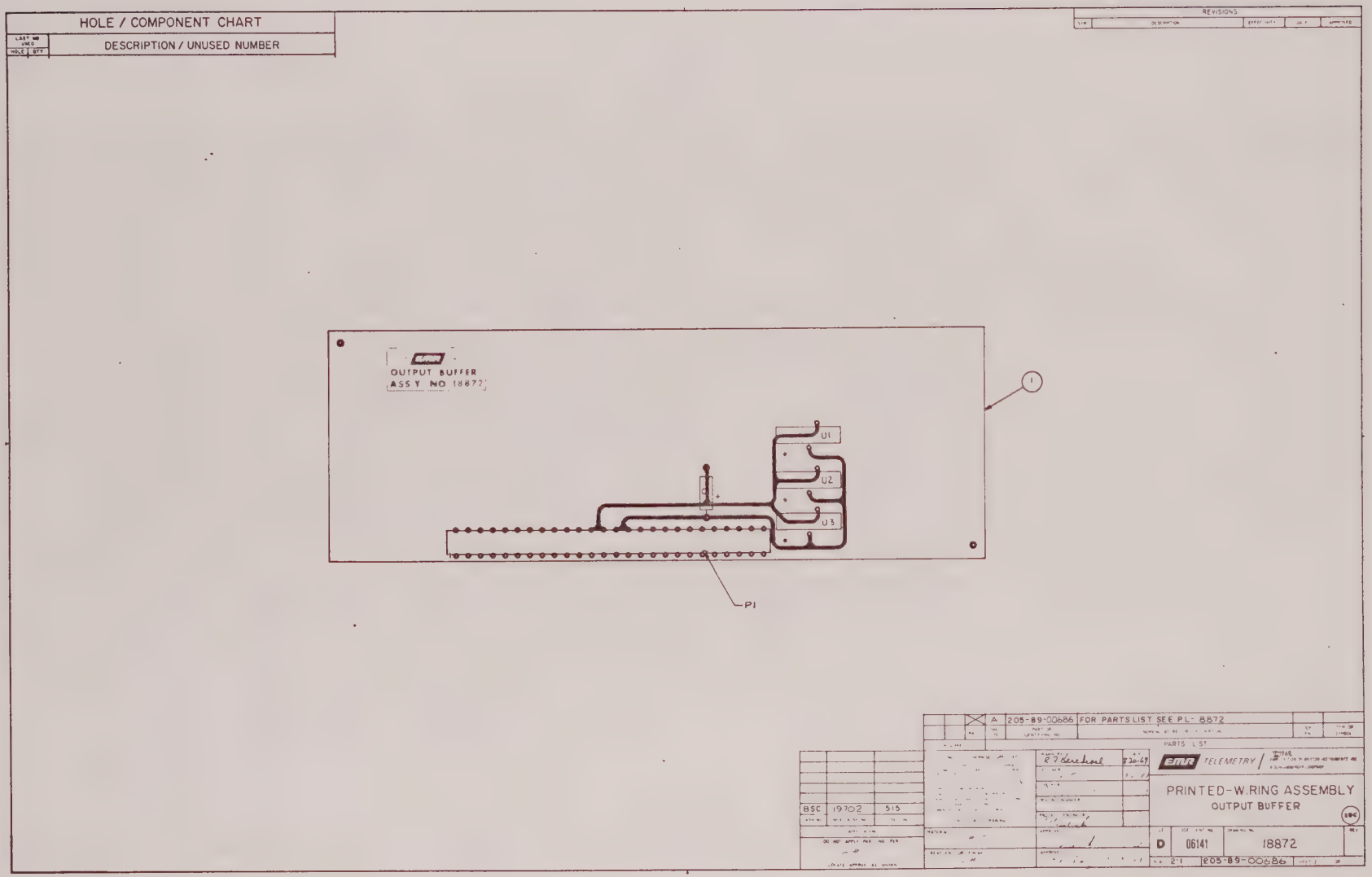


Figure 5-4. Output Buffer Printed-Wiring Board Assembly Diagram

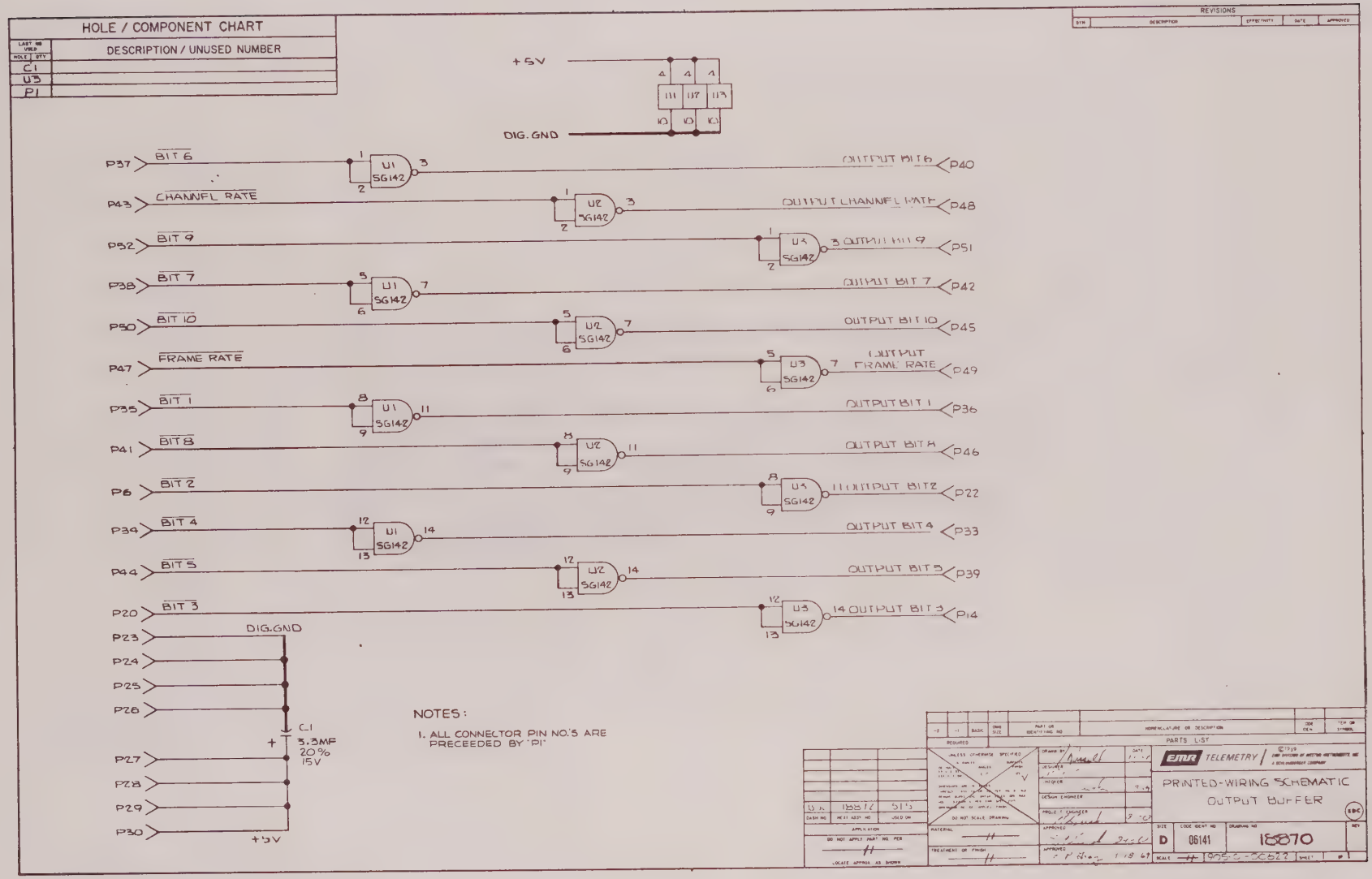


Figure 5-5. Output Buffer Printed-Wiring Board Schematic Diagram

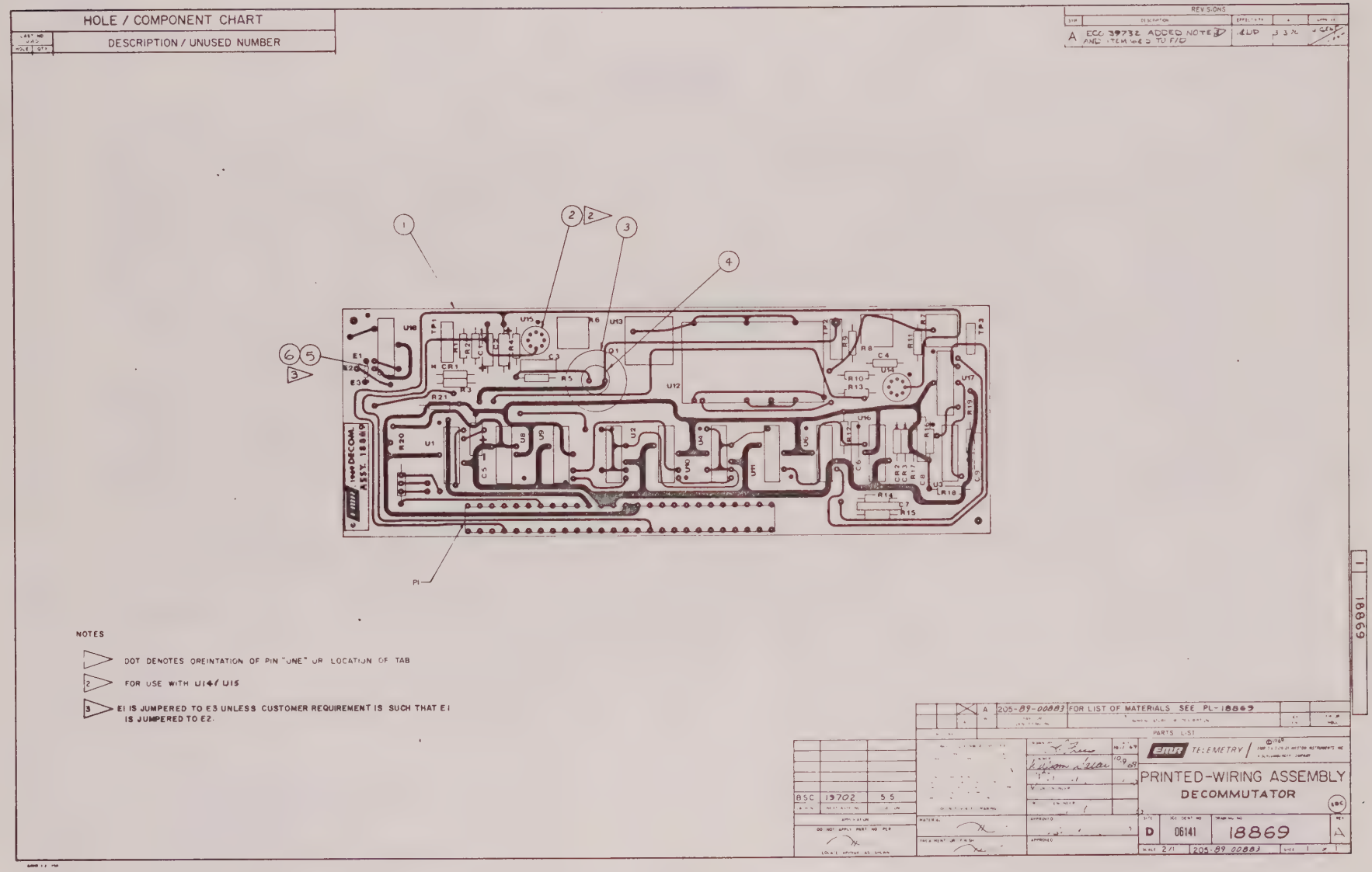


Figure 5-6. Decommutator Printed-Wiring Board Assembly Diagram

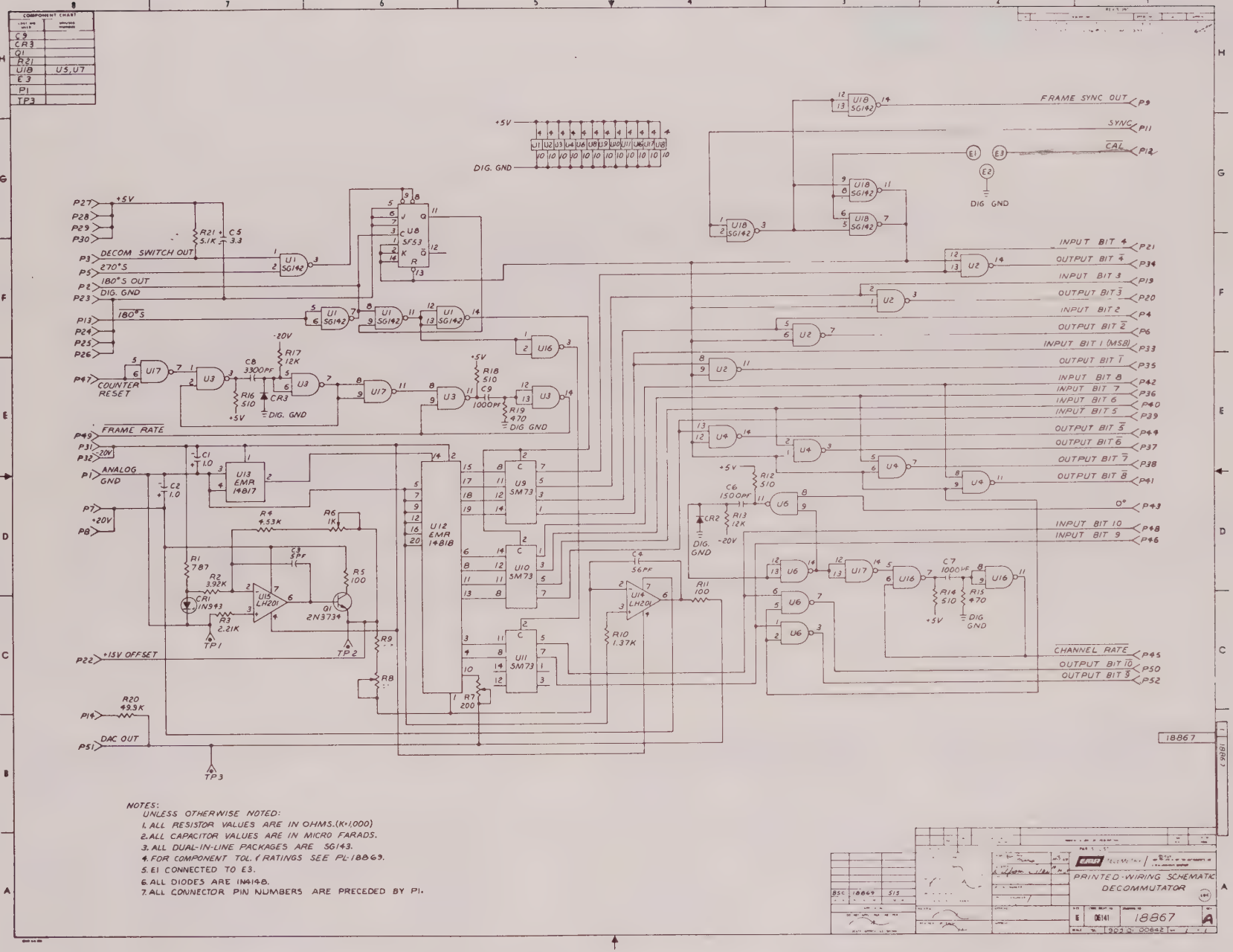
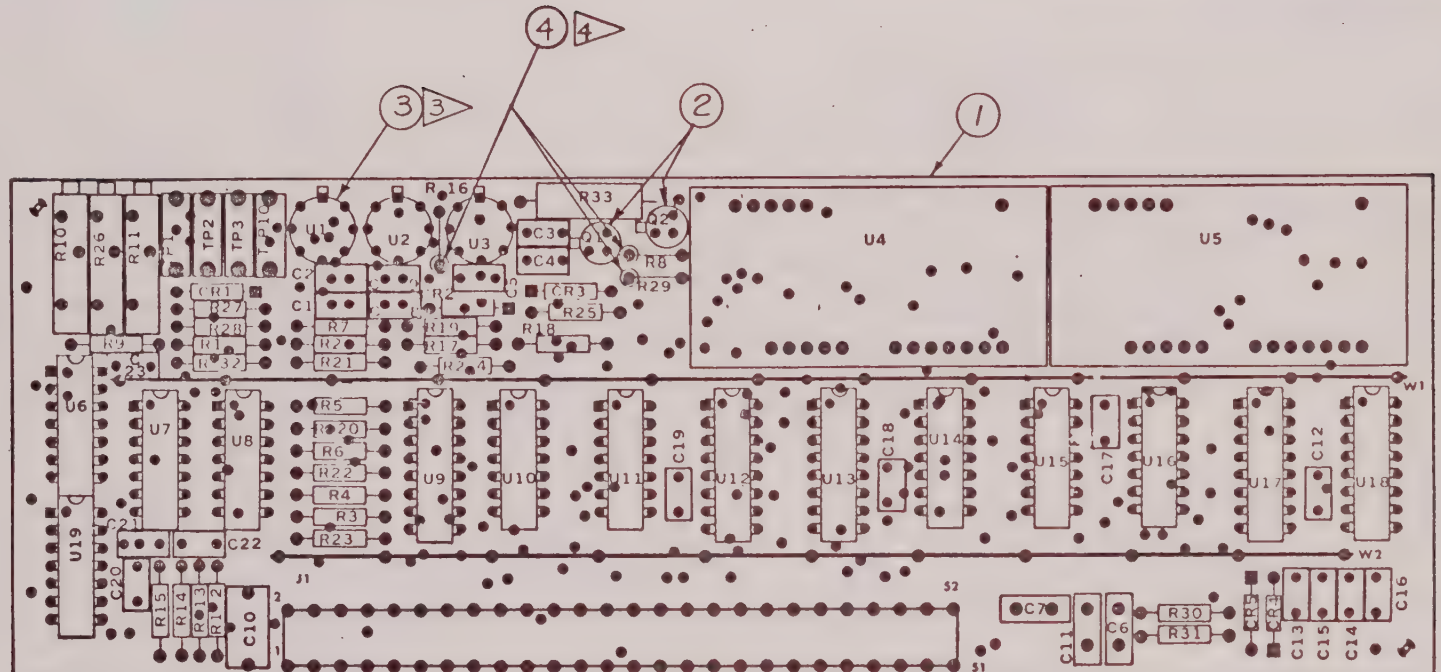


Figure 5-7. Decommutator Printed-Wiring Board Schematic Diagram

HOLE	QTY.	DESCRIPTION/UNUSED NUMBER

REVISION			
A	RCD CHG REDESIGNED	1 & UP	11/11/74
B	ECO 50632, INTRIM REV U9 BUS		10/10/74
C	ECO 50668, MOVED U6 & U19 UP		10/15/74
D	ECO 50919 (INTRIM)		11/26/74
E	ECO 50920 U9 PWR CHGD		11/26/74



28090

4. INSTALL R8, R16 & R29 IN STAND UP POSITION. INSTALL ITEM 4 AS REQ D

3. FOR USE WITH U1, U2 AND U3.

2. ■ SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES.

1. MAX HEIGHT: A. COMPONENT SIDE .400.
B. NON-COMPONENT SIDE .093.

UNLESS OTHERWISE SPECIFIED:
NOTES:

GRADE	CATEGORY	SIMILAR TO
II	II	

DASH NO	NEXT ASSY NO	USED ON
BSC	19072	515

APPLICATION

DO NOT APPLY PART NO
IDENTIFY PER EMR 13406

LOCATE APPROX AS SHOWN

CONFIGURATION	BASIC	CONTROL NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	ITEM OR SYMBOL
		205-89-01594	PL-280.IC	FOR PARTS LIST, SEE PL-28090	

QTY REQUIRED

PARTS LIST

UNLESS OTHERWISE SPECIFIED
TOLERANCES: DECIMALS .XX ± .03, .XXX ± .010; ANGLES ± 1/2°; SURFACE FINISH 125
DIMENSIONS ARE IN INCHES
THREADS CLASS 2A OR 2B PER MIL-S-7742
REMOVE BURRS AND BREAK EDGES .020 MAX.
HOLE TOLERANCES PER EMR SPEC 2876
DIMENSIONS INCLUDE APPLIED FINISH
EMR WORKMANSHIP STANDARDS APPLY
DO NOT SCALE DRAWING

MATERIAL

TREATMENT OR FINISH

		DATE
DRAWN BY	T K Briggs	7/11/74
DESIGNED	T K Briggs	7/11/74
CHECKER	RON BASHAM	2/29/74
DESIGN ENGINEER		
PROJECT ENGINEER	JACK BISHOP	2/29/74
APPROVED	R L Bush	7/15/74
APPROVED		

EMR Schlumberger
EMR TELEMETRY
WESTON INSTRUMENTS INC
SARASOTA FLORIDA 33578

PWA,
SERVO DAC

SIZE	CODE IDENT NO.	DRAWING NO.
C	06141	28090

SCALE 2/1 | 205-89-01594 | SHEET 1 OF 1

Figure 5-8. Servo DAC Printed-Wiring Board Assembly Diagram

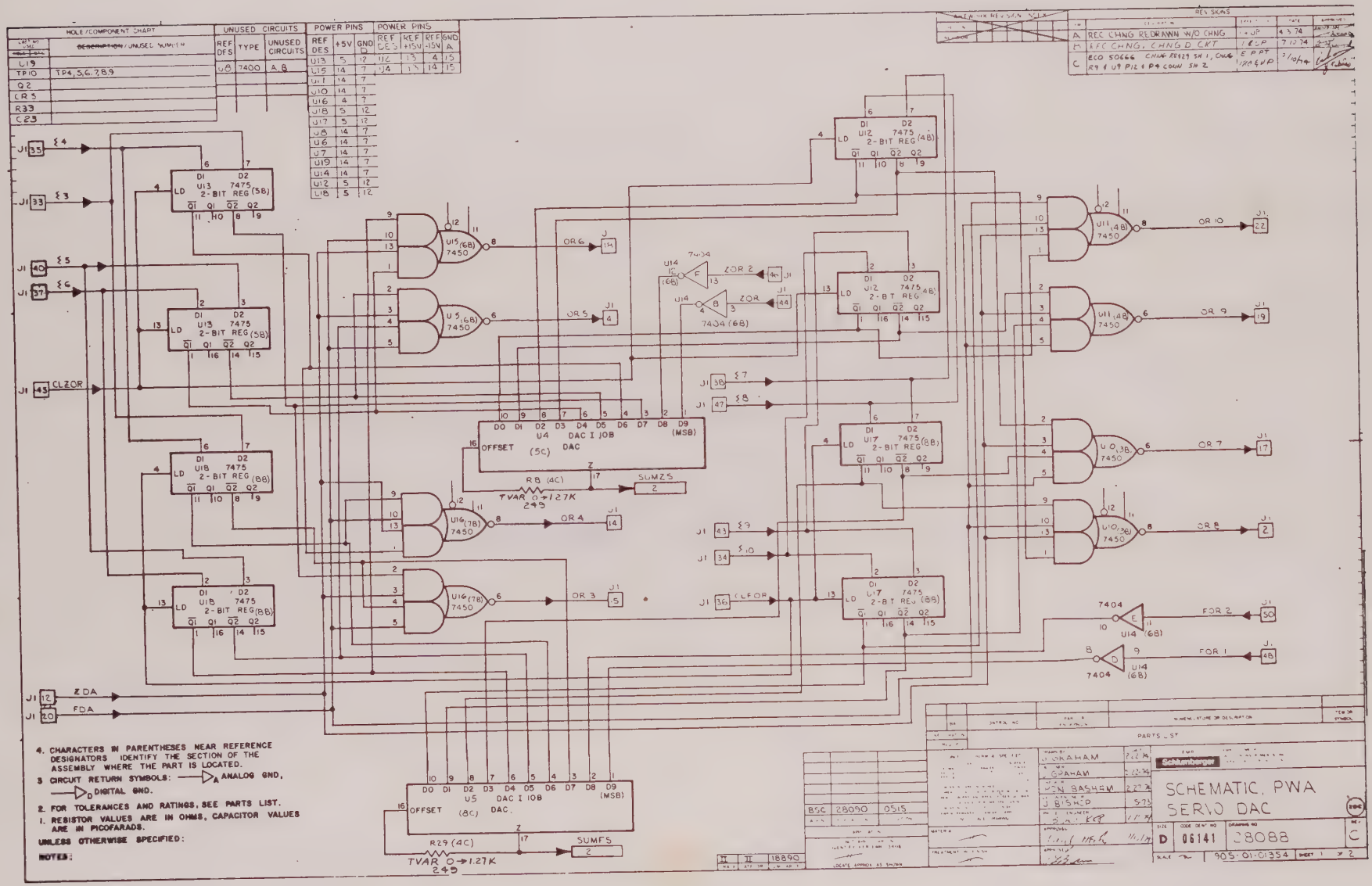


Figure 5-9. Servo DAC Printed-Wiring Board Schematic Diagram

(Sheet 1 of 2)

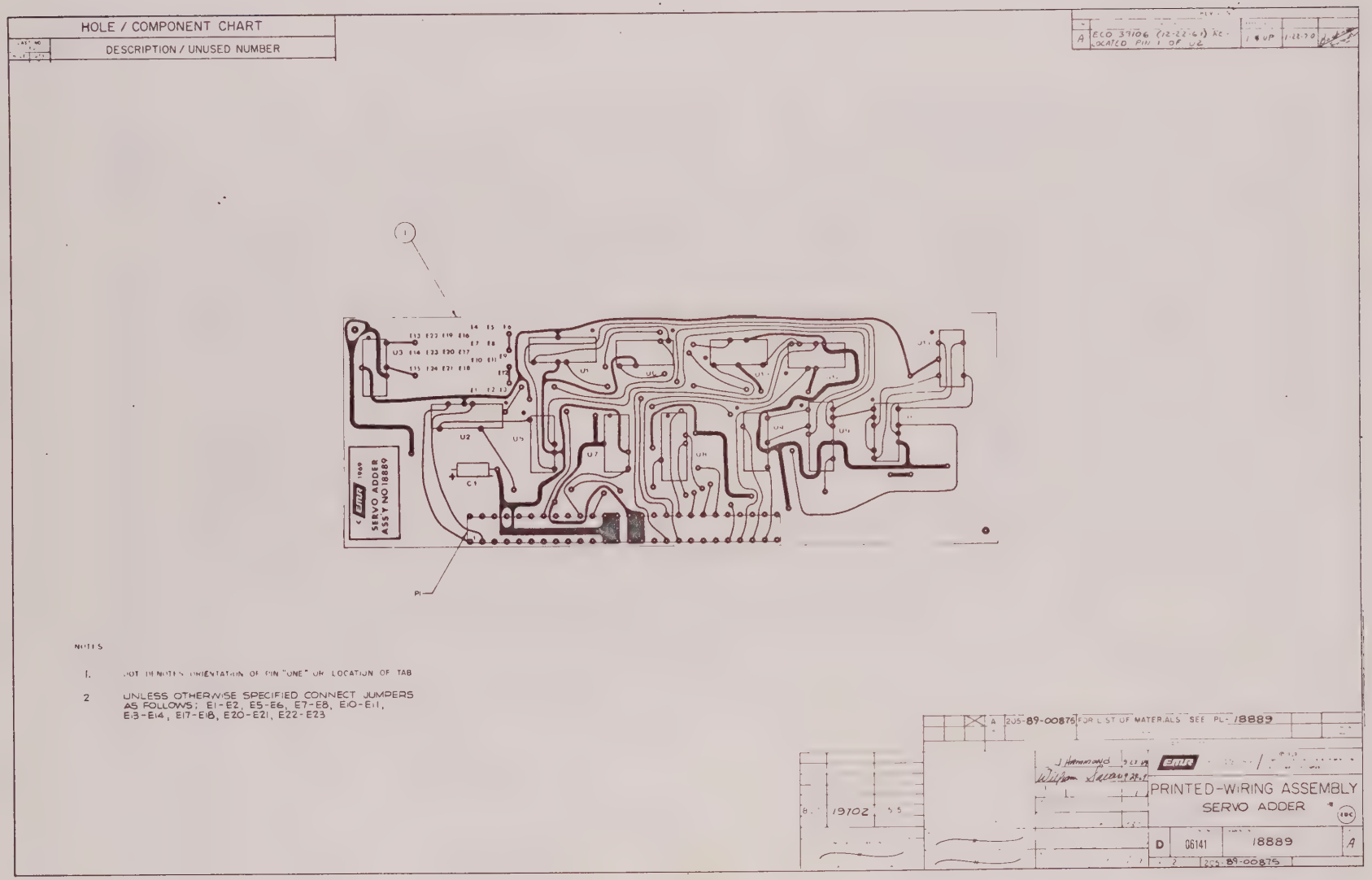


Figure 5-10. Servo Adder Printed-Wiring Board Assembly Diagram

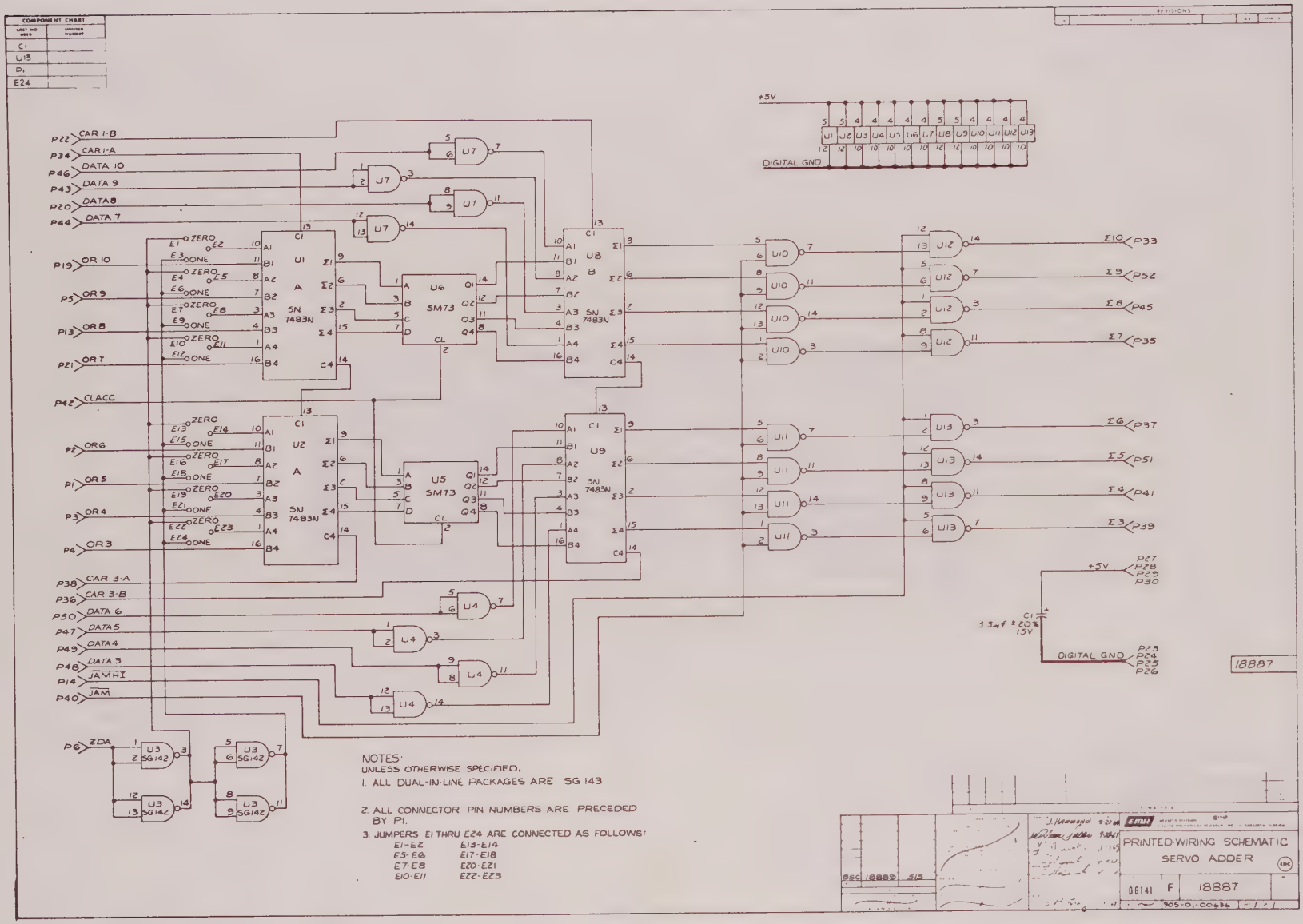


Figure 5-11. Servo Adder Printed-Wiring Board Schematic Diagram

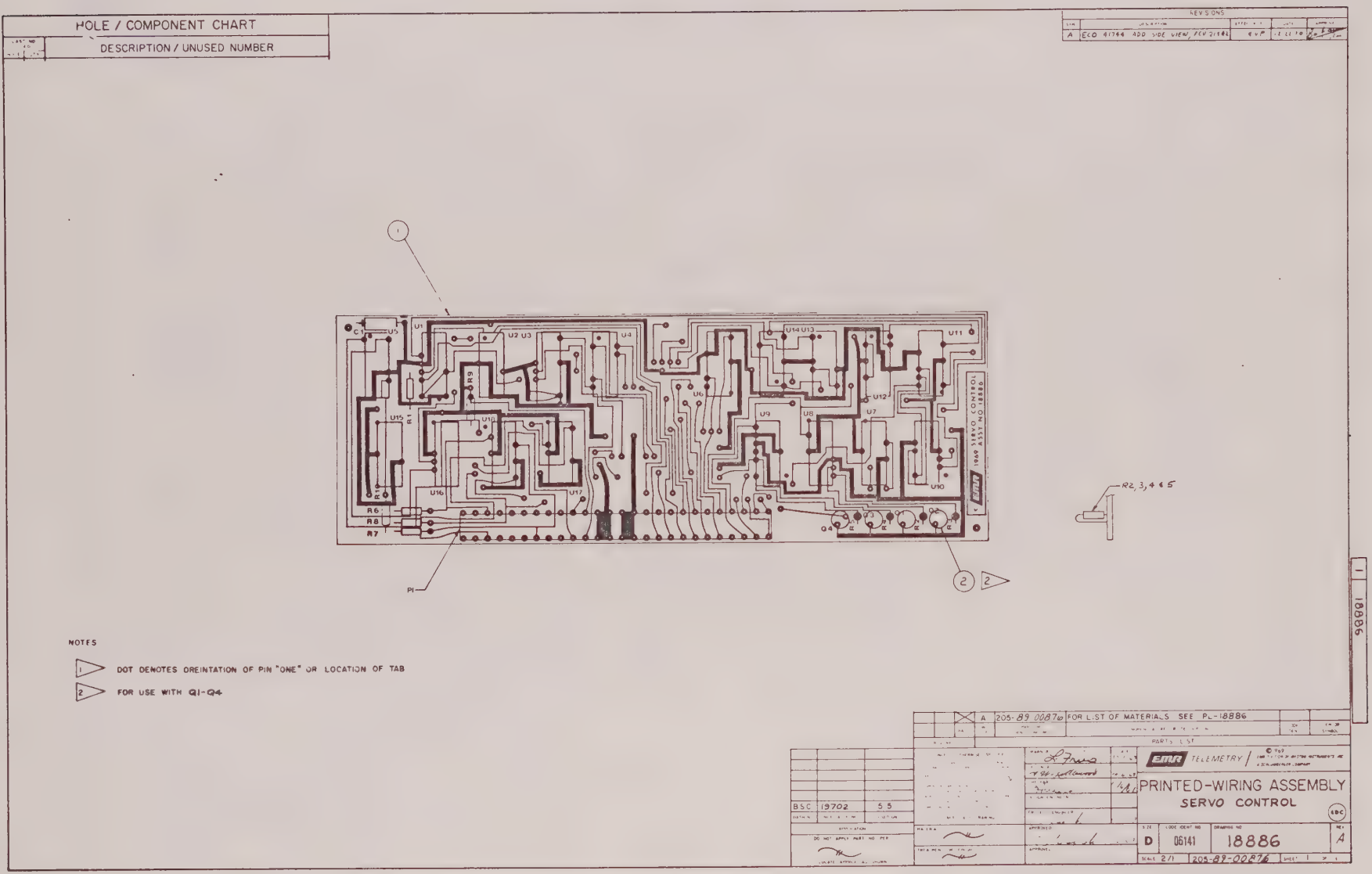


Figure 5-12. Servo Control Printed-Wiring Board Assembly Diagram

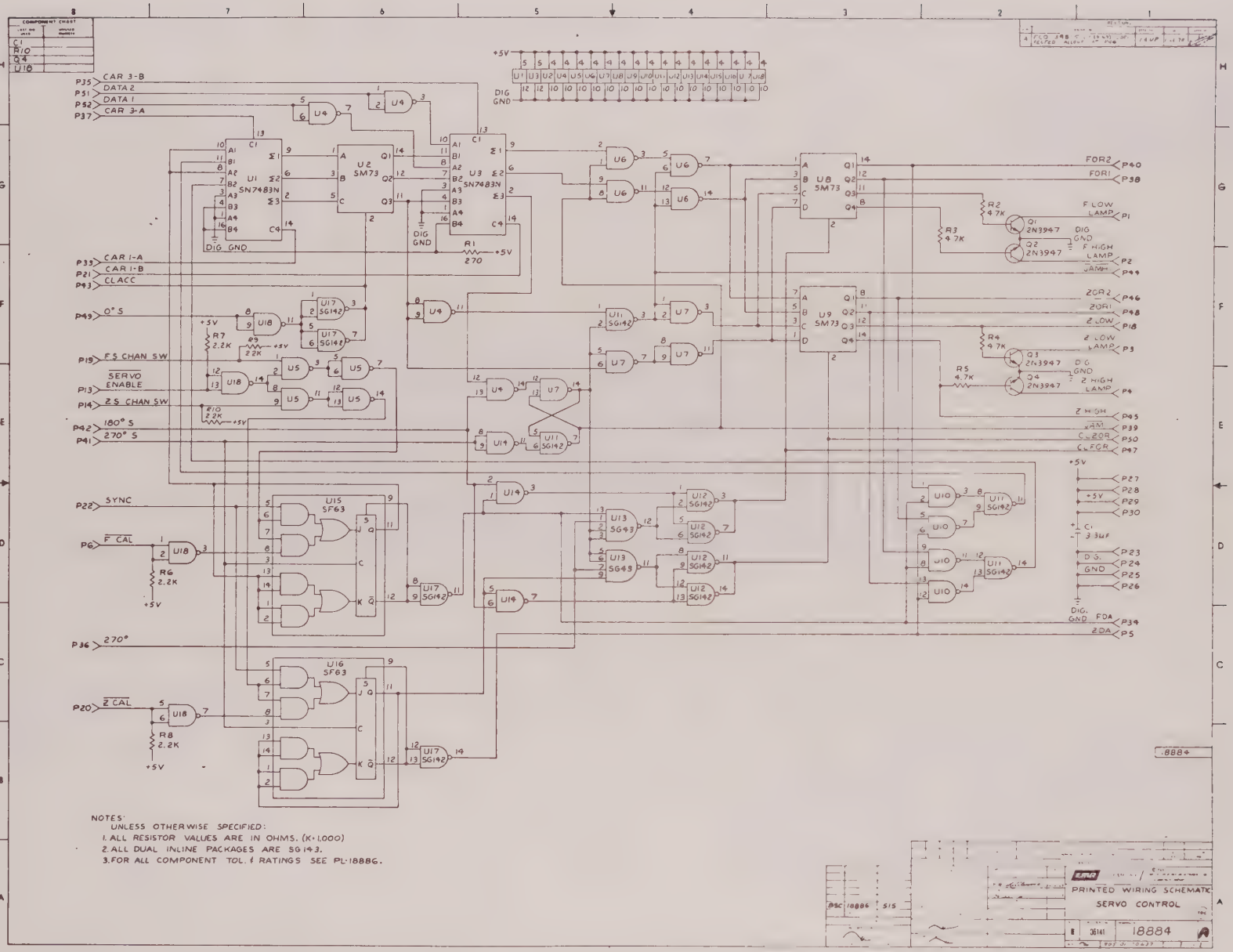


Figure 5-13. Servo Control Printed-Wiring Board Schematic Diagram

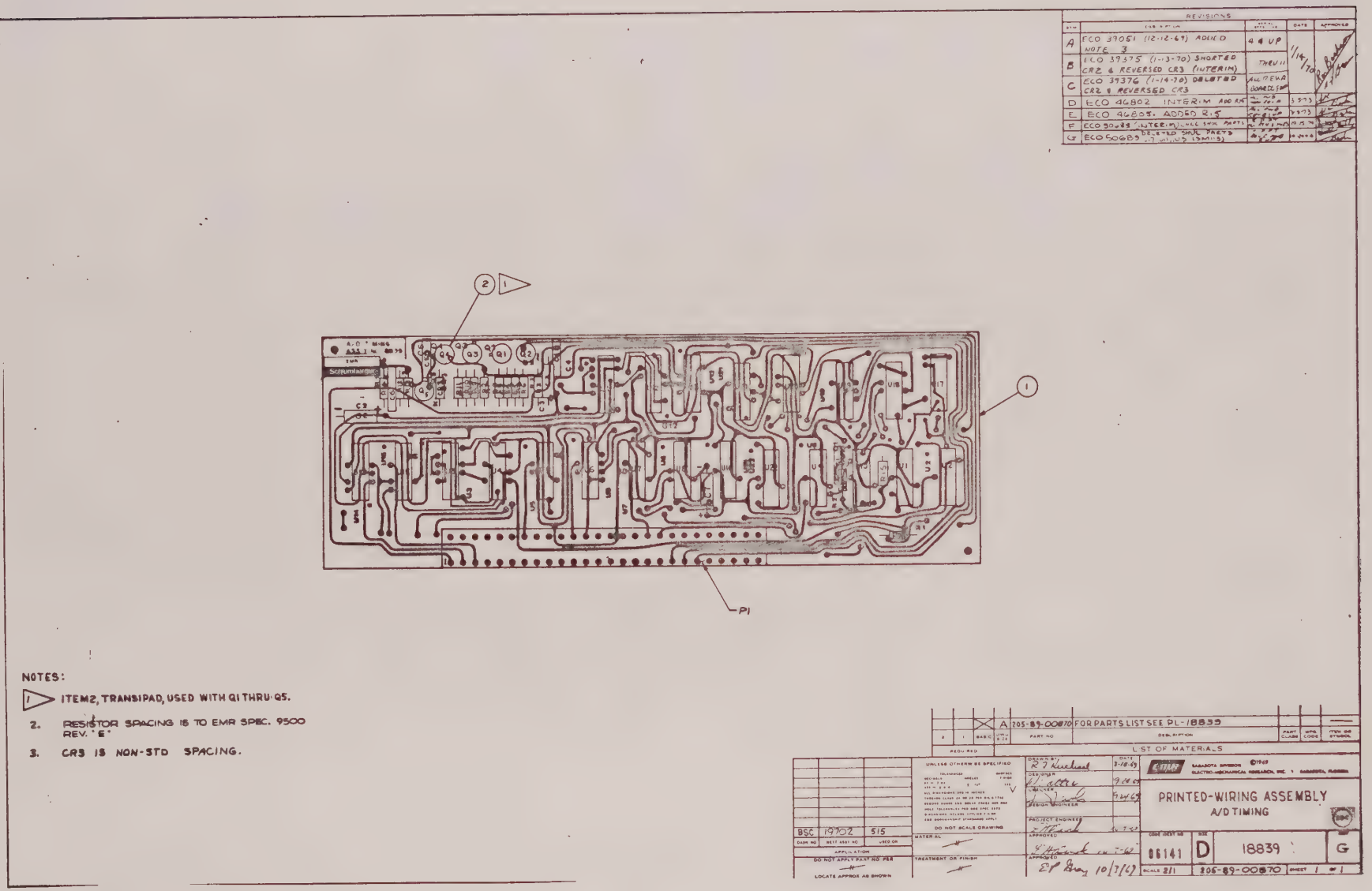


Figure 5-14. A/D Timing Printed-Wiring Board Assembly Diagram

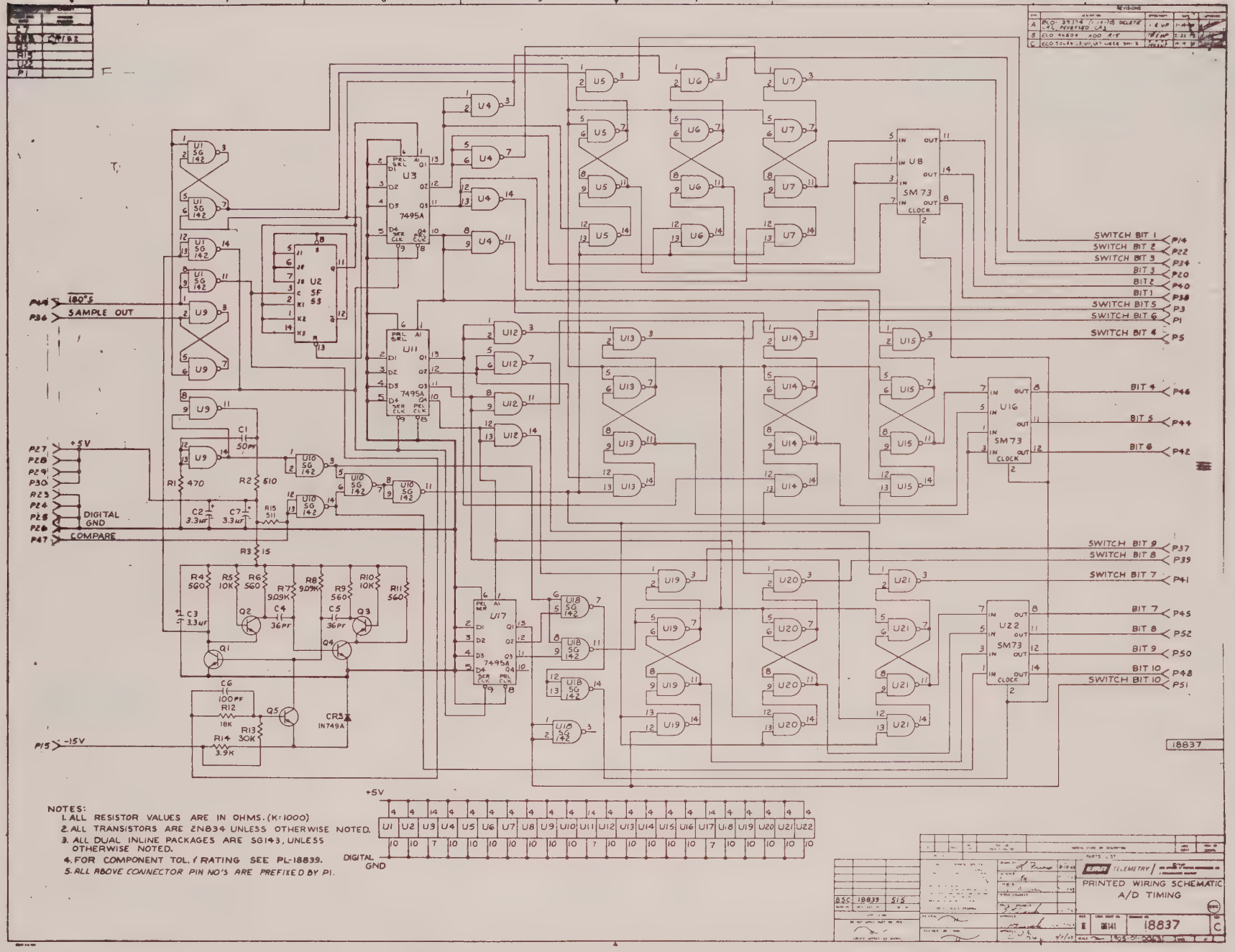


Figure 5-15. A/D Timing Printed-Wiring Board Schematic Diagram

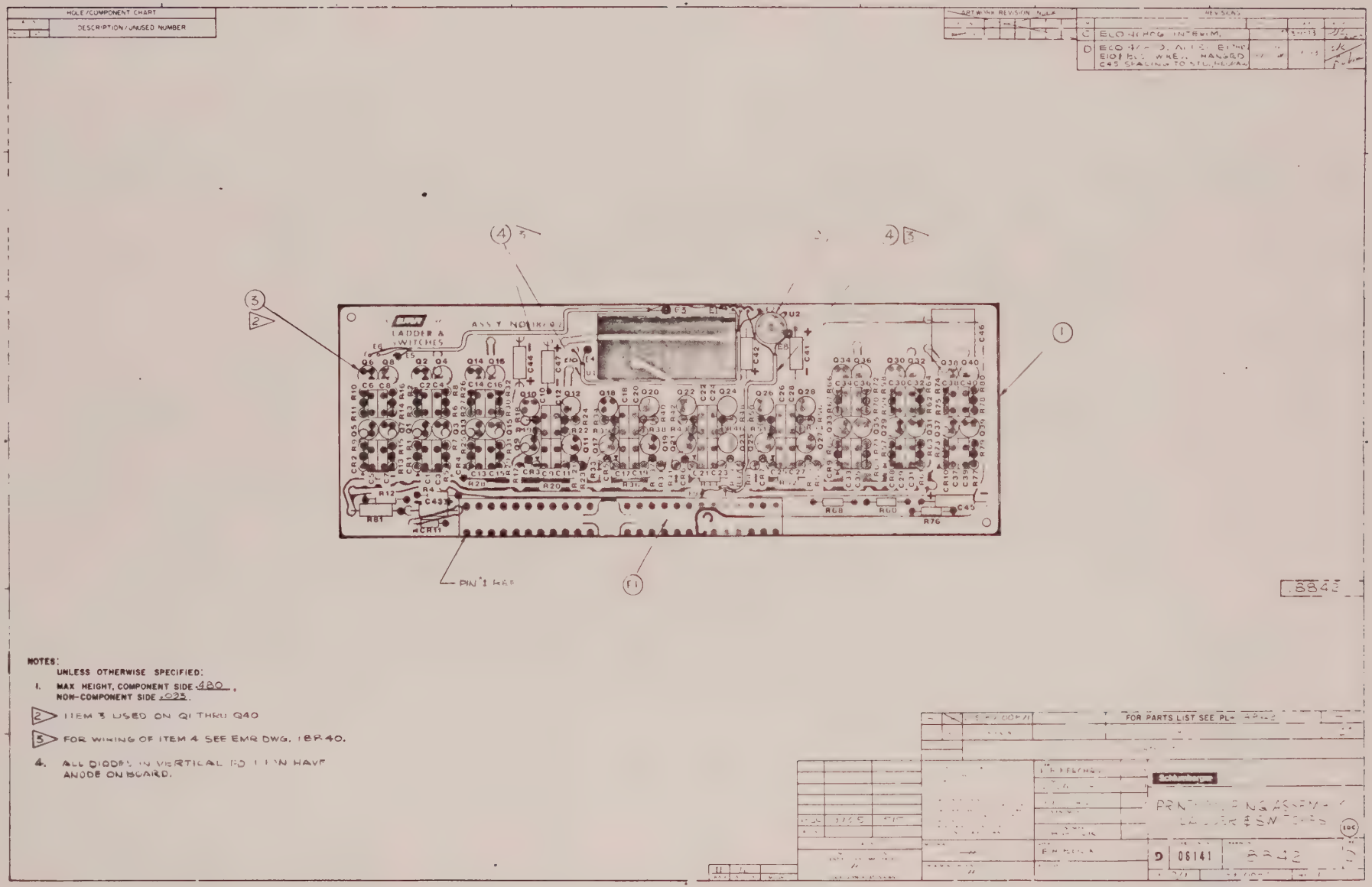


Figure 5-16. Ladder and Switches Printed-Wiring Board Assembly Diagram

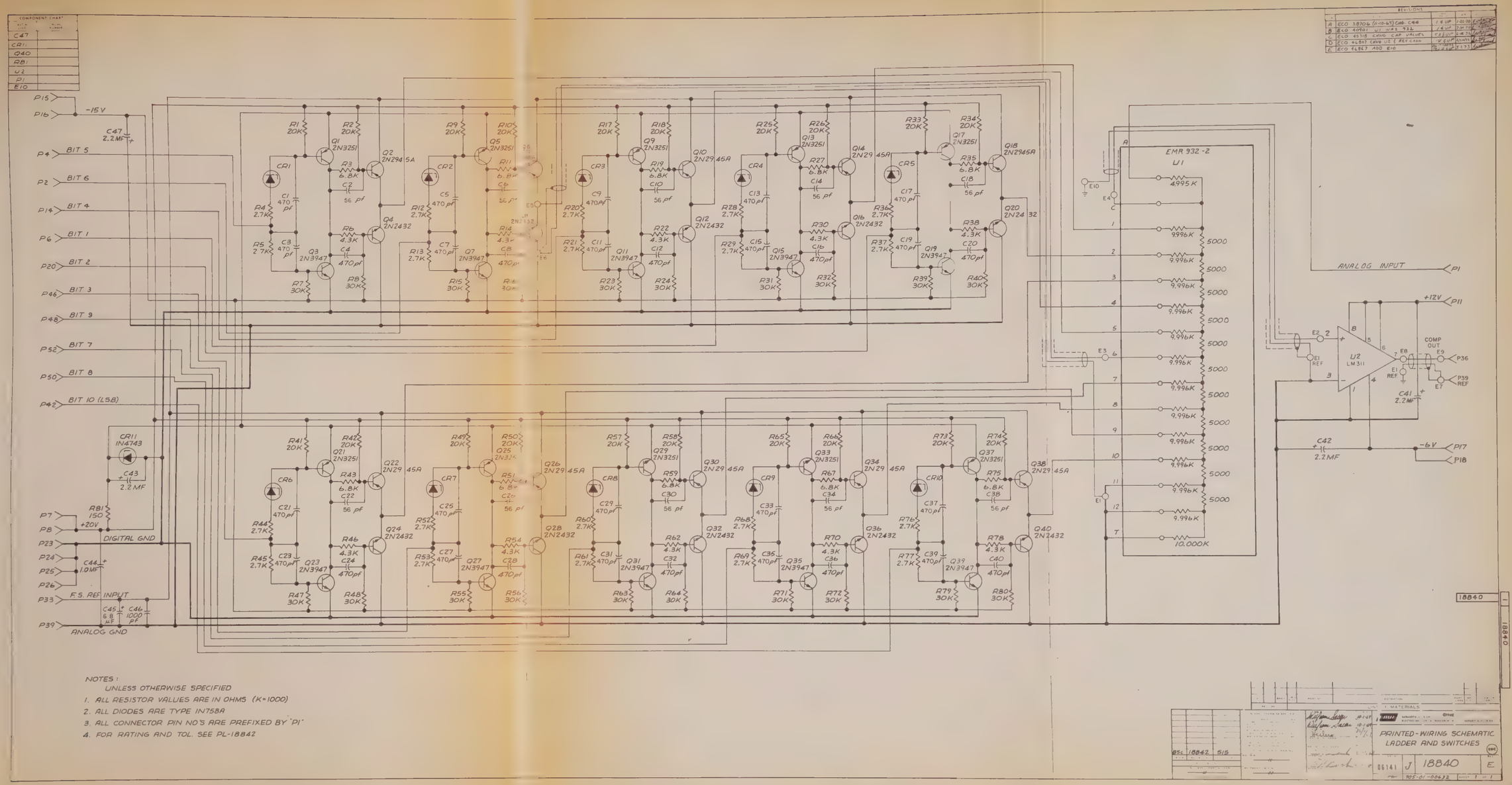


FIGURE 5-17. LADDER AND SWITCHES PRINTED-WIRING BOARD SCHEMATIC DIAGRAM

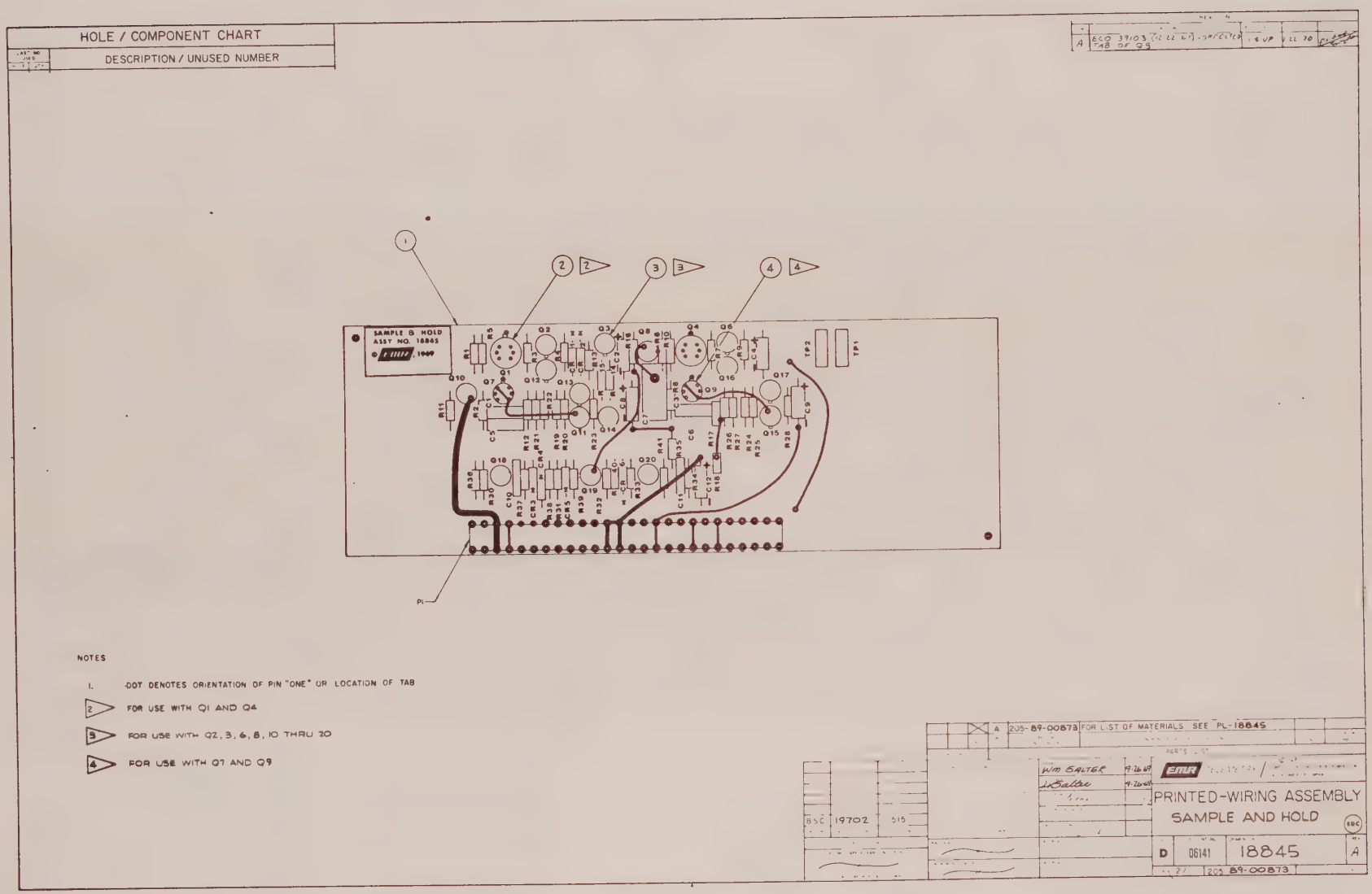


Figure 5-18. Sample and Hold Printed-Wiring Board Assembly Diagram

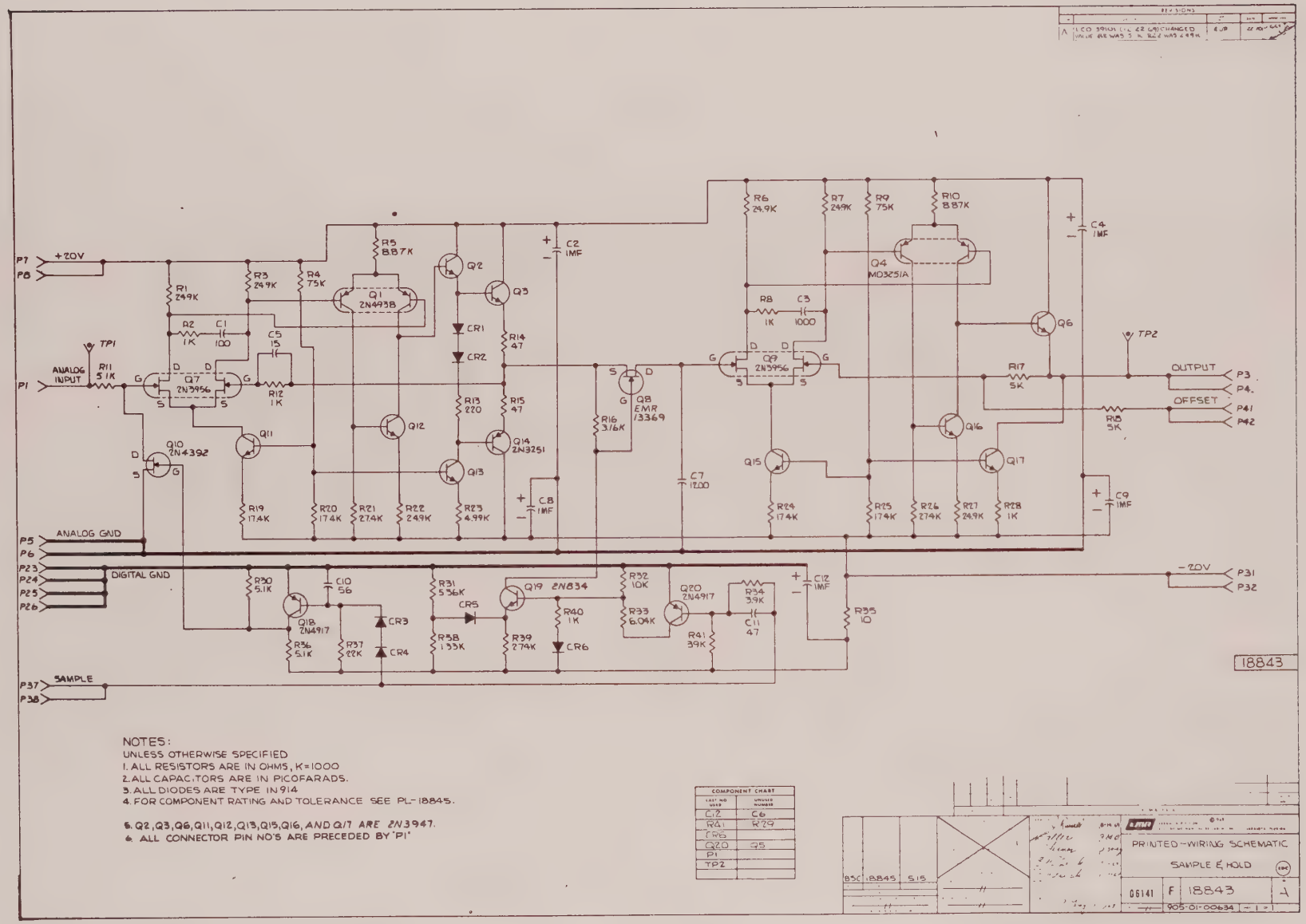
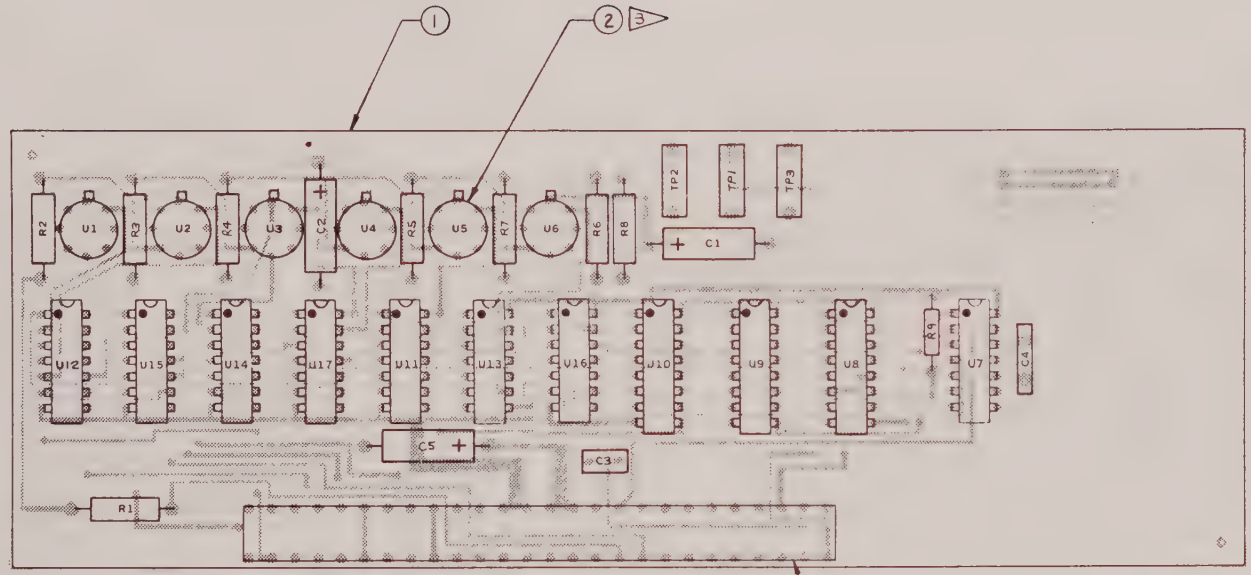


Figure 5-19. Sample and Hold Printed-Wiring Board Schematic Diagram



NOTES:

UNLESS OTHERWISE SPECIFIED:

1. MAX HEIGHT. COMPONENT SIDE .525 .
   NON-COMPONENT SIDE .093 .

2 ■ SQUARE PAD INDICATES (+) POSITIVE END OF CAPACITORS, CATHODE END OF DIODES AND MECHANICAL ORIENTATION OF SYMMETRICAL MULTI-LEADED DEVICES.

3 USE ITEM 2 WITH U1 THRU U6

REVISIONS

SYM	DESCRIPTION	SERIAL EFFECTIVE	DATE	APPROVED

		X	A	205-89-01272	FOR PARTS LIST SEE PL-22852	—	—	—
		BASIC	REV LTR	PART NO	DESCRIPTION	PART CLASS	MFG CODE	ITEM OR SYMBOL

REQUIRED — LIST OF MATERIALS

BSC	19702	515
DASH NO	NEXT ASSY NO	USED ON

APPLICATION

DO NOT APPLY PART NO PER

LOCATE APPROX AS SHOWN

UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING

MATERIAL

TREATMENT OR FINISH

DRAWN BY	J. Russell	DATE 2/9/72
DESIGNER	Dwight Dupree	2/9/72
CHECKER		
DESIGN ENGINEER		
PROJECT ENGINEER	J. Bishop	2/11/72
APPROVED		

EDR TELEMETRY DIVISION
ELECTRO-MECHANICAL RESEARCH, INC. • SARASOTA, FLORIDA

PRINTED WIRING ASSEMBLY, FRAME SYNC RECOGNITION (EDC)

CODE IDENT NO	SIZE		REV
06141	C	22852	
SCALE 2/1	205-89-01272	SHEET 1 OF 1	

Figure 5-20. Frame Sync Recognition Printed-Wiring Board Assembly Diagram

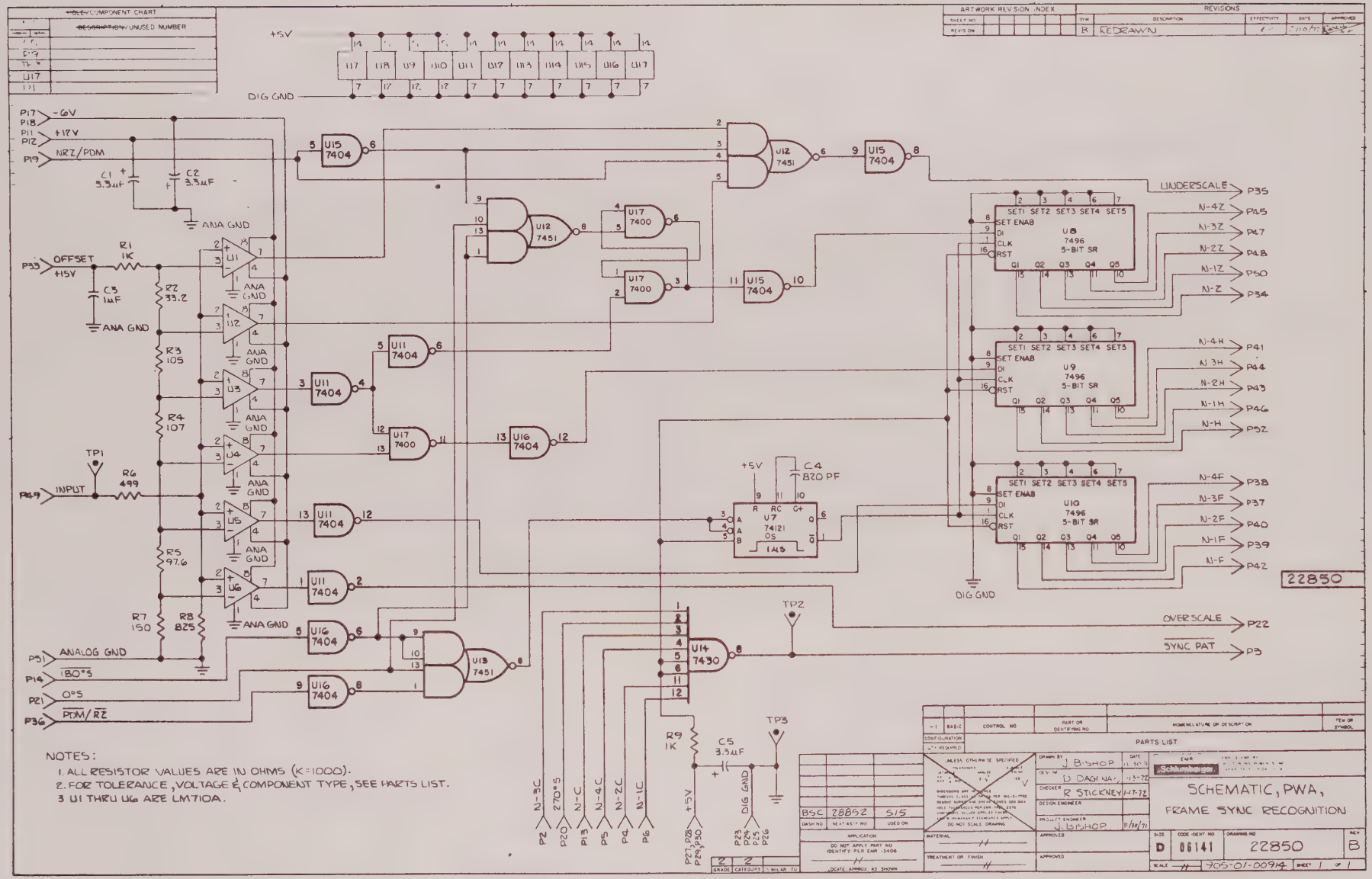


Figure 5-21. Frame Sync Recognition Printed-Wiring Board Schematic Diagram

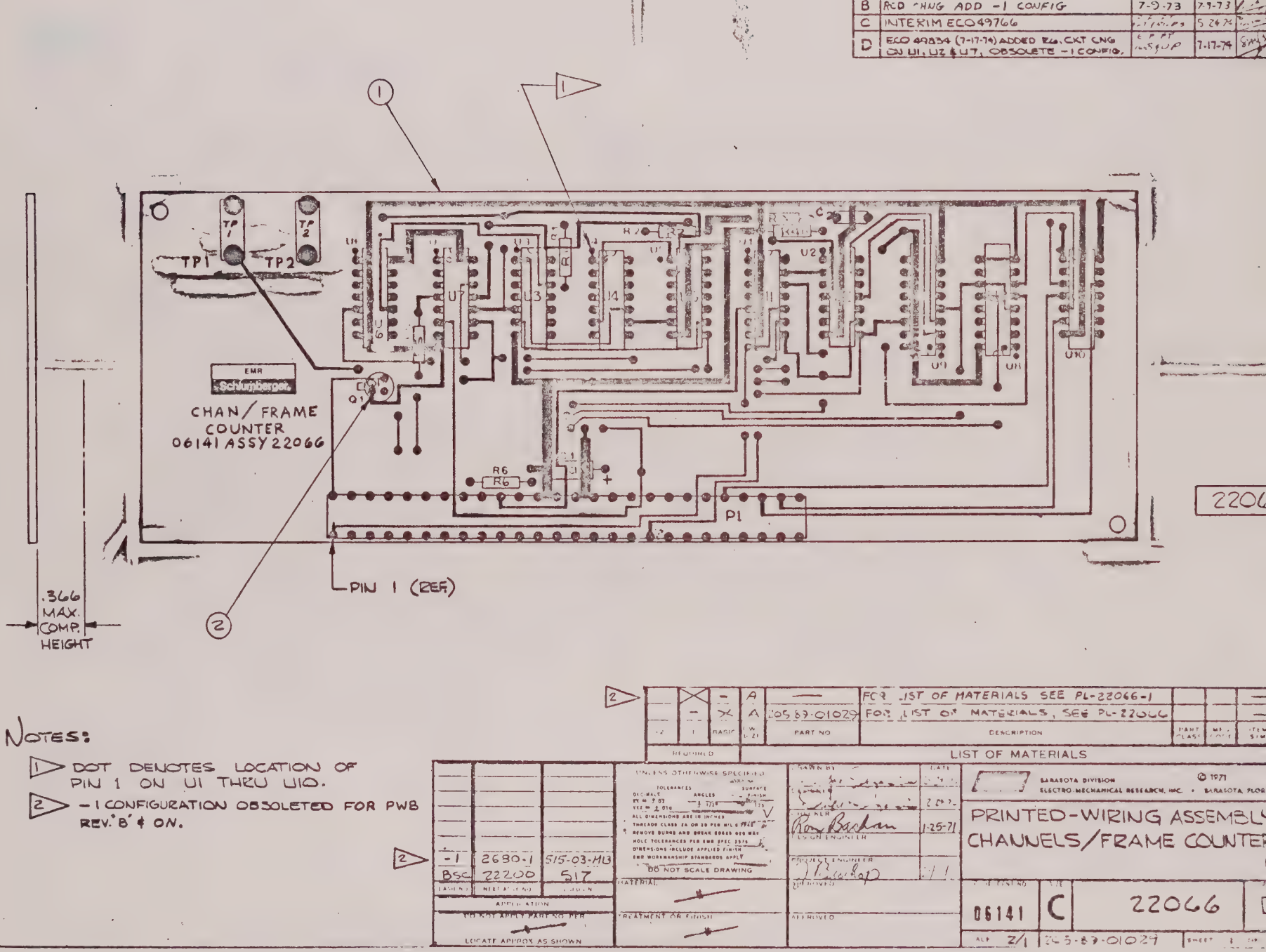


Figure 5-22. Channels/Frame Counter Printed-Wiring Board Assembly Diagram

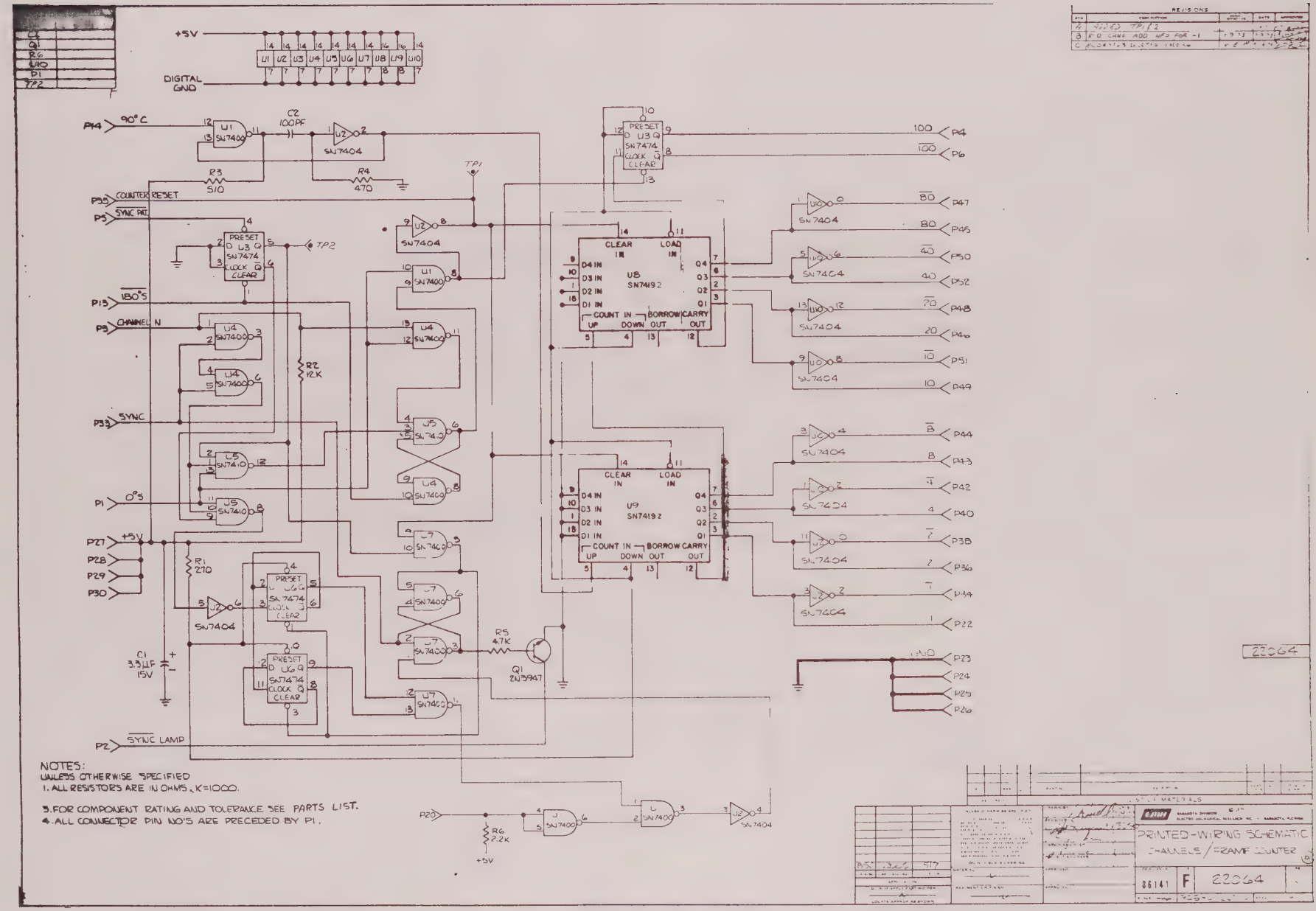


Figure 5-23. Channels/Frame Counter Printed-Wiring Board Logic/Schematic Diagram

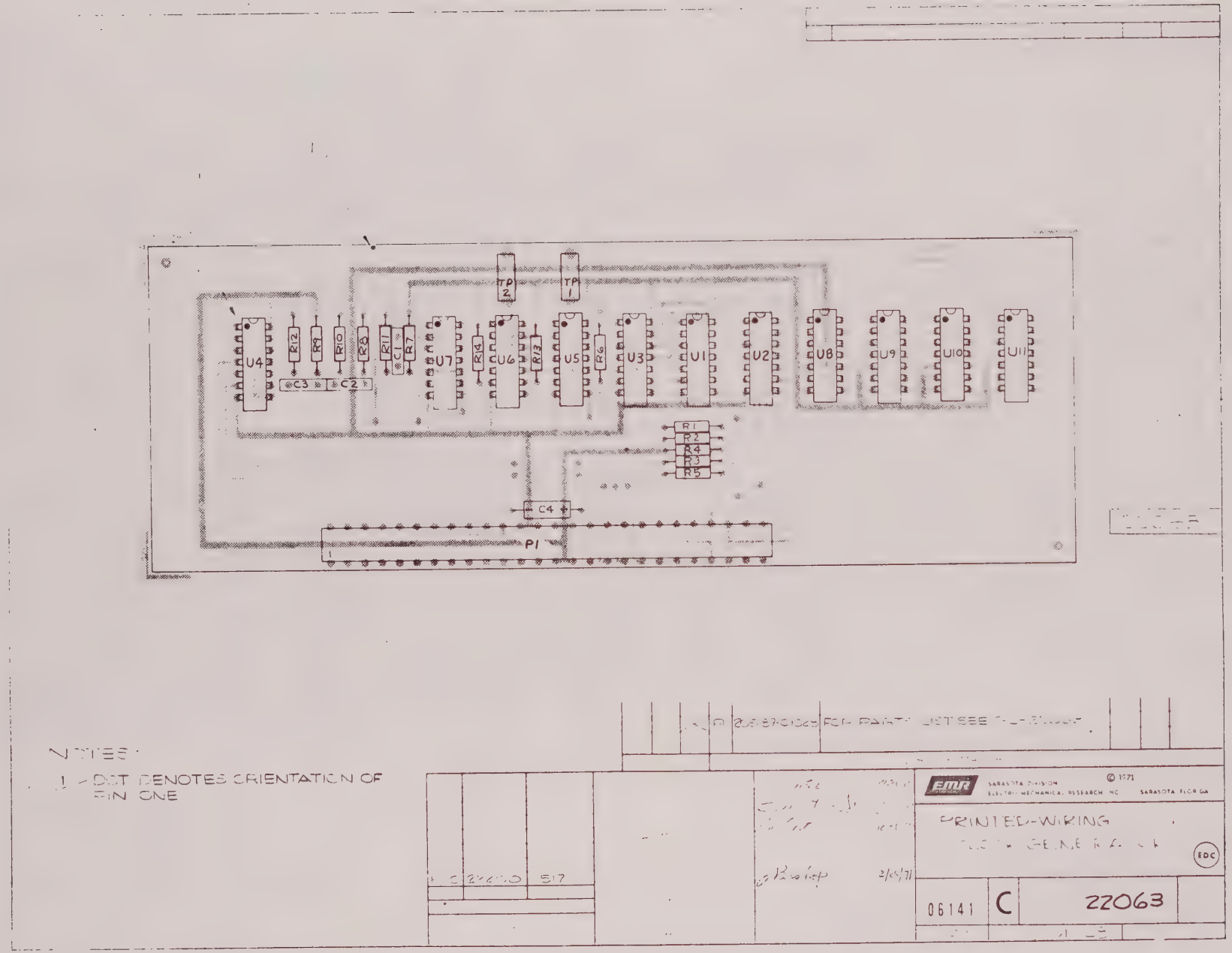


Figure 5-24. Clock Generator Printed-Wiring Board Assembly Diagram

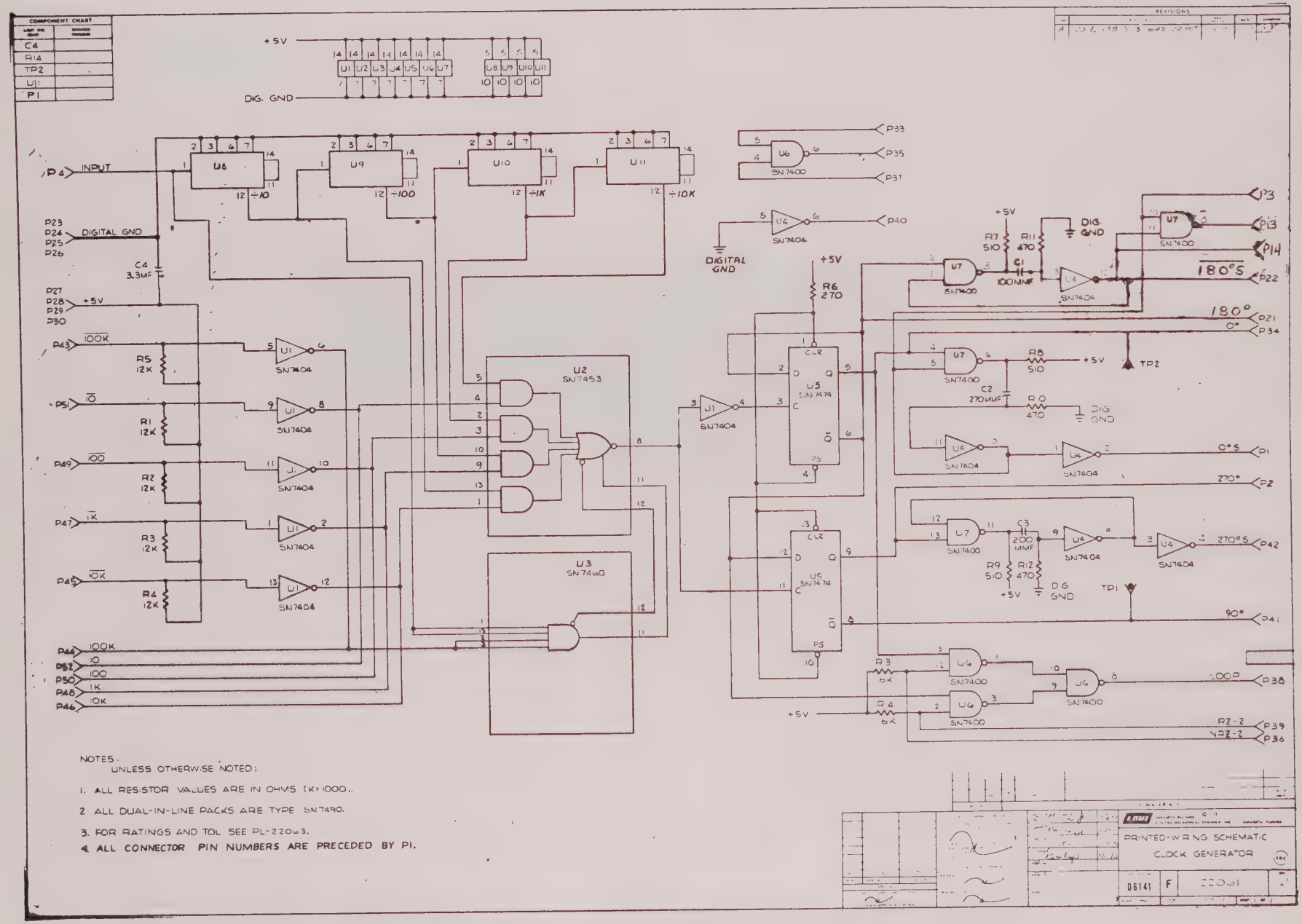


Figure 5-25. Clock Generator Printed-Wiring Board Logic/Schematic Diagram

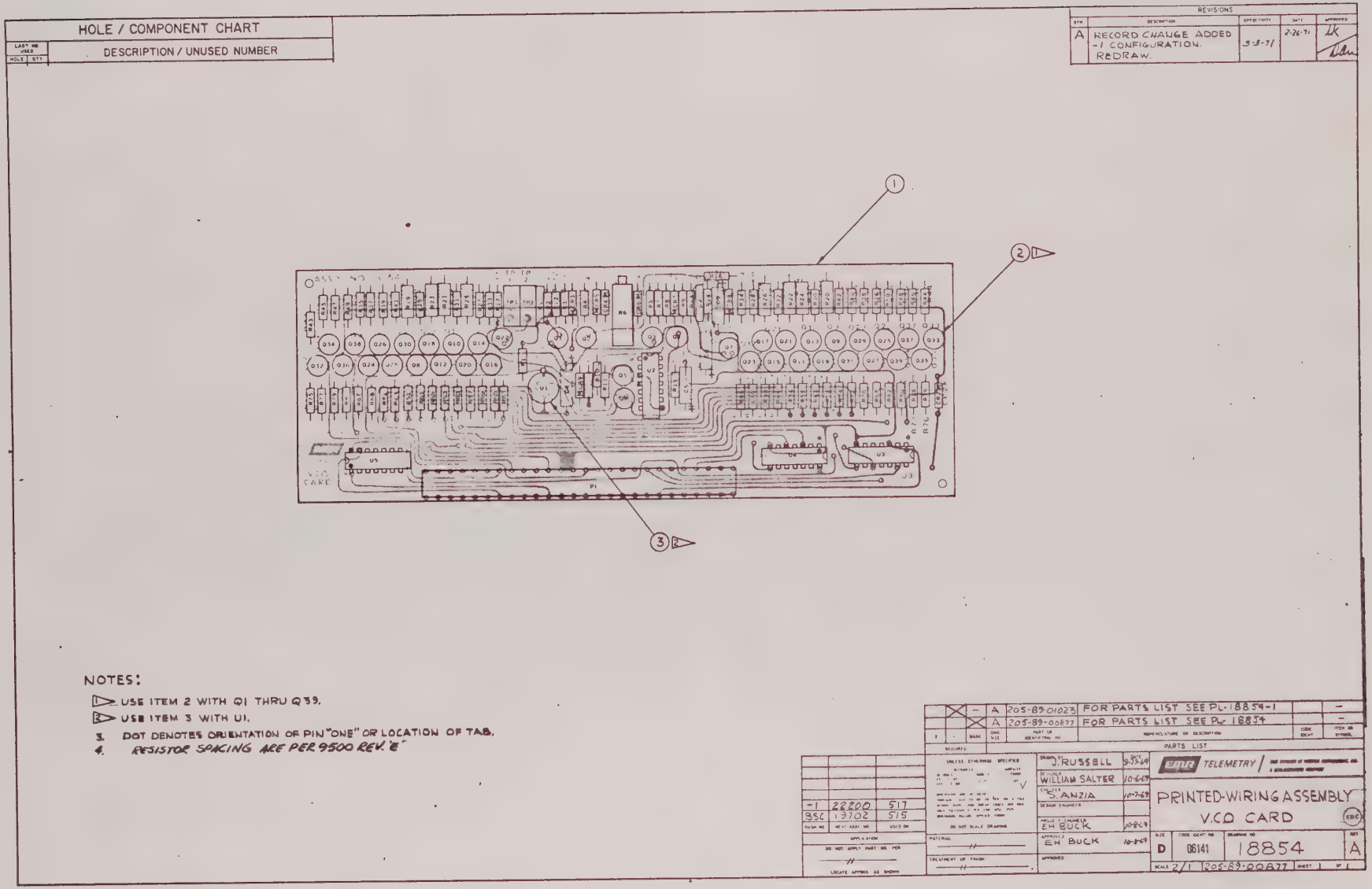


Figure 5-26. VCO Printed-Wiring Board Assembly Diagram

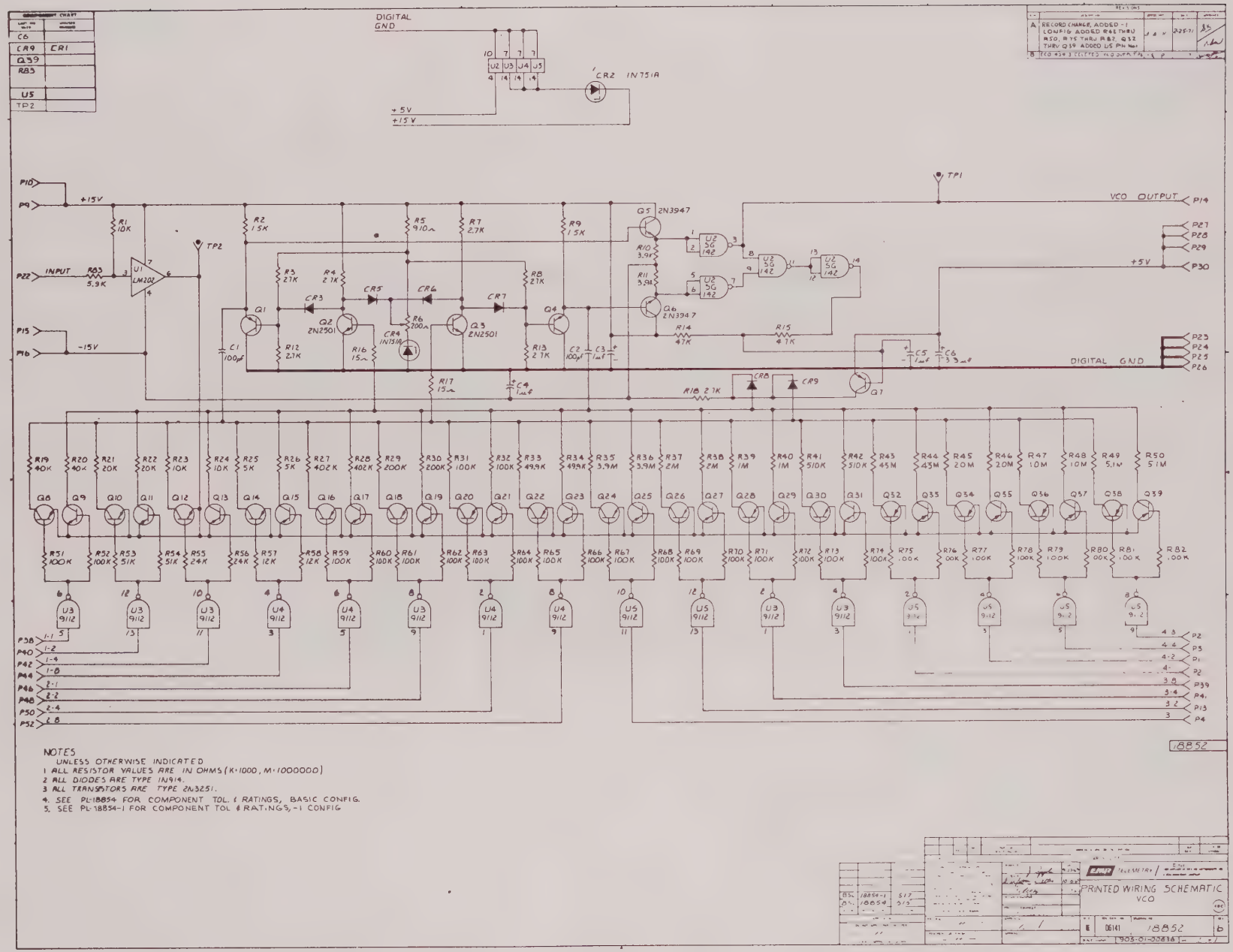


Figure 5-27. VCO Printed-Wiring Board Schematic Diagram

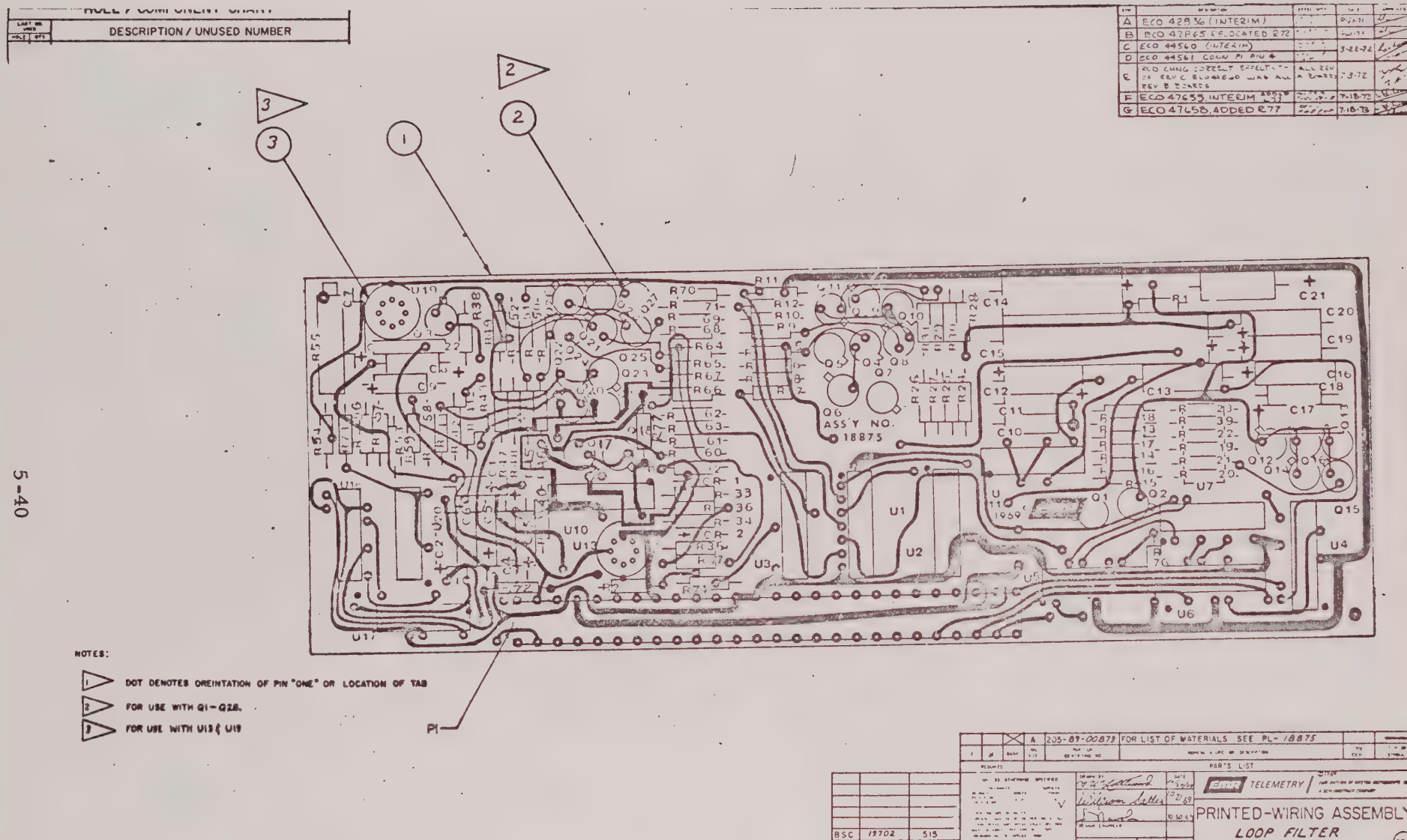


Figure 5-28. Loop Filter Printed-Wiring Board Assembly Diagram

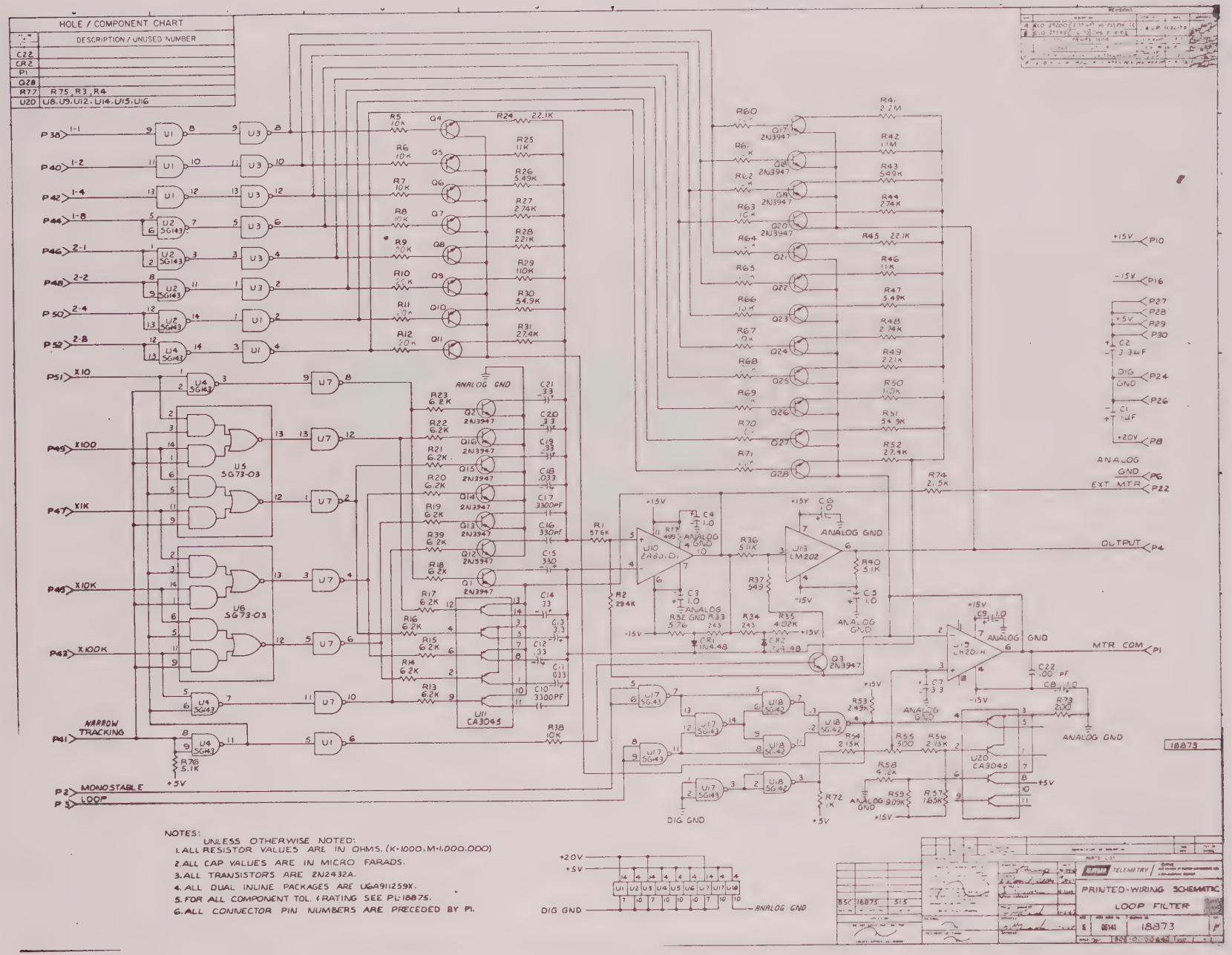


Figure 5-29. Loop Filter Printed-Wiring Board Schematic Diagram

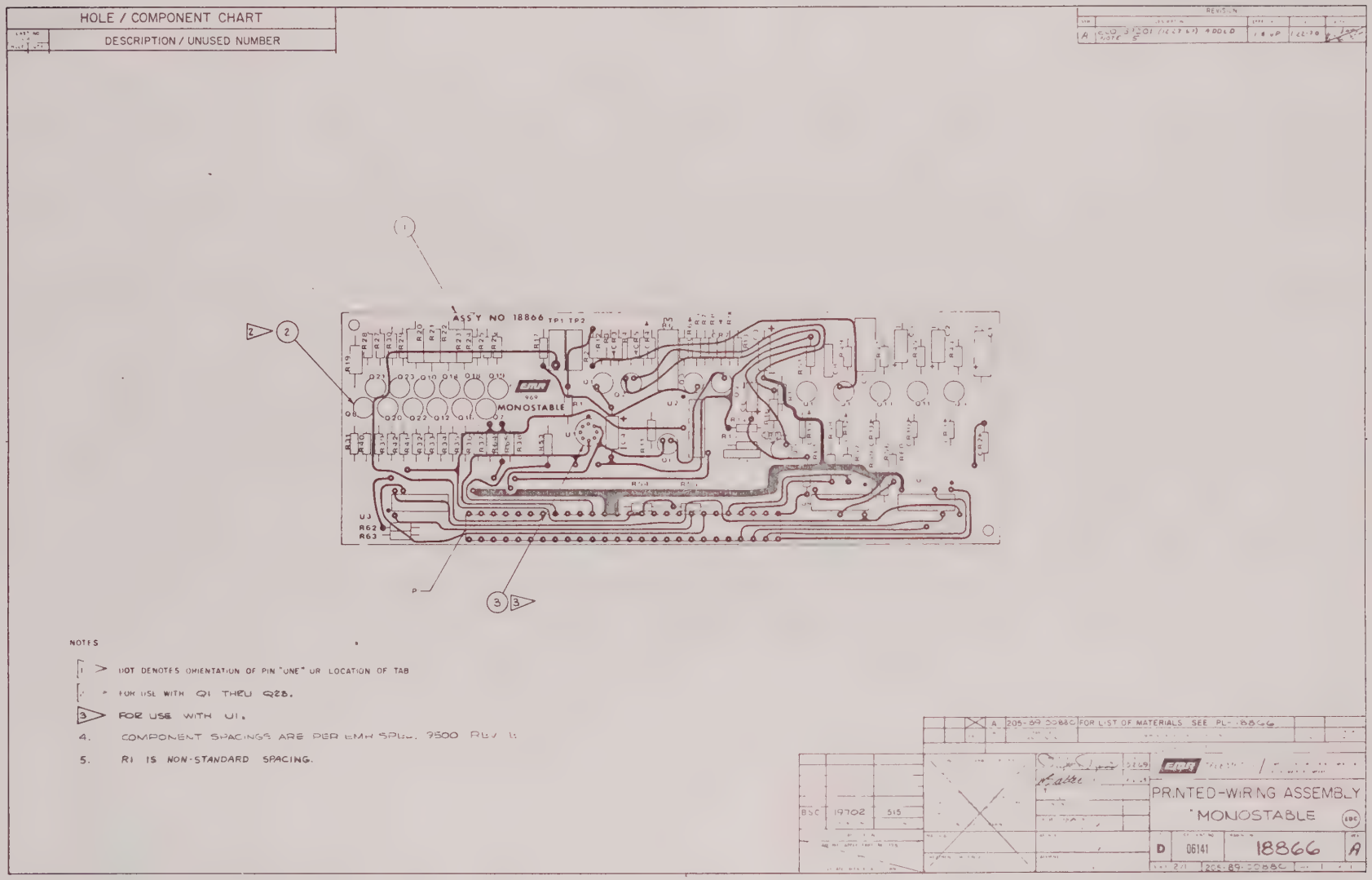


Figure 5-30. Monostable Printed-Wiring Board Assembly Diagram

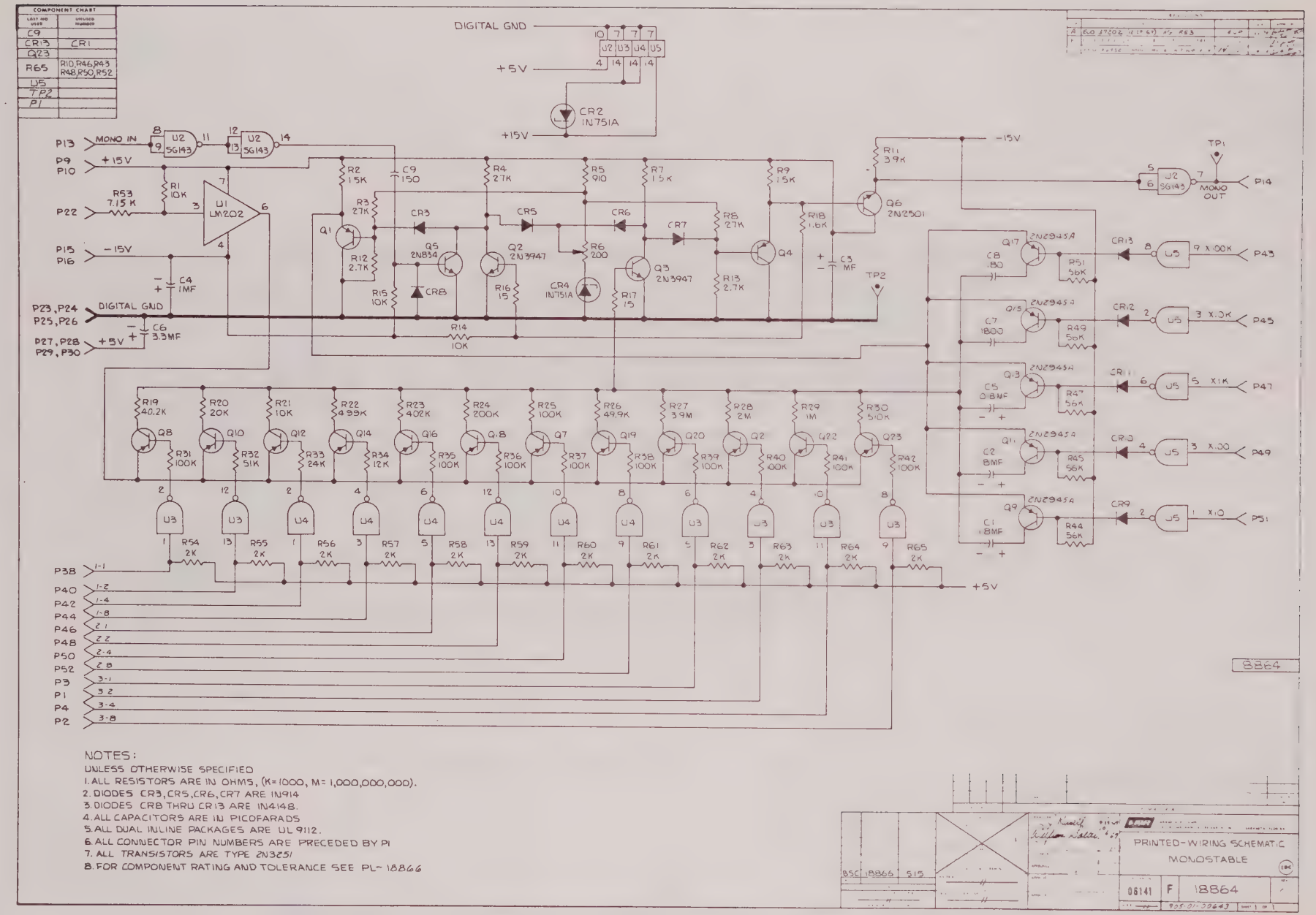


Figure 5-31. Monostable Printed-Wiring Board Schematic Diagram

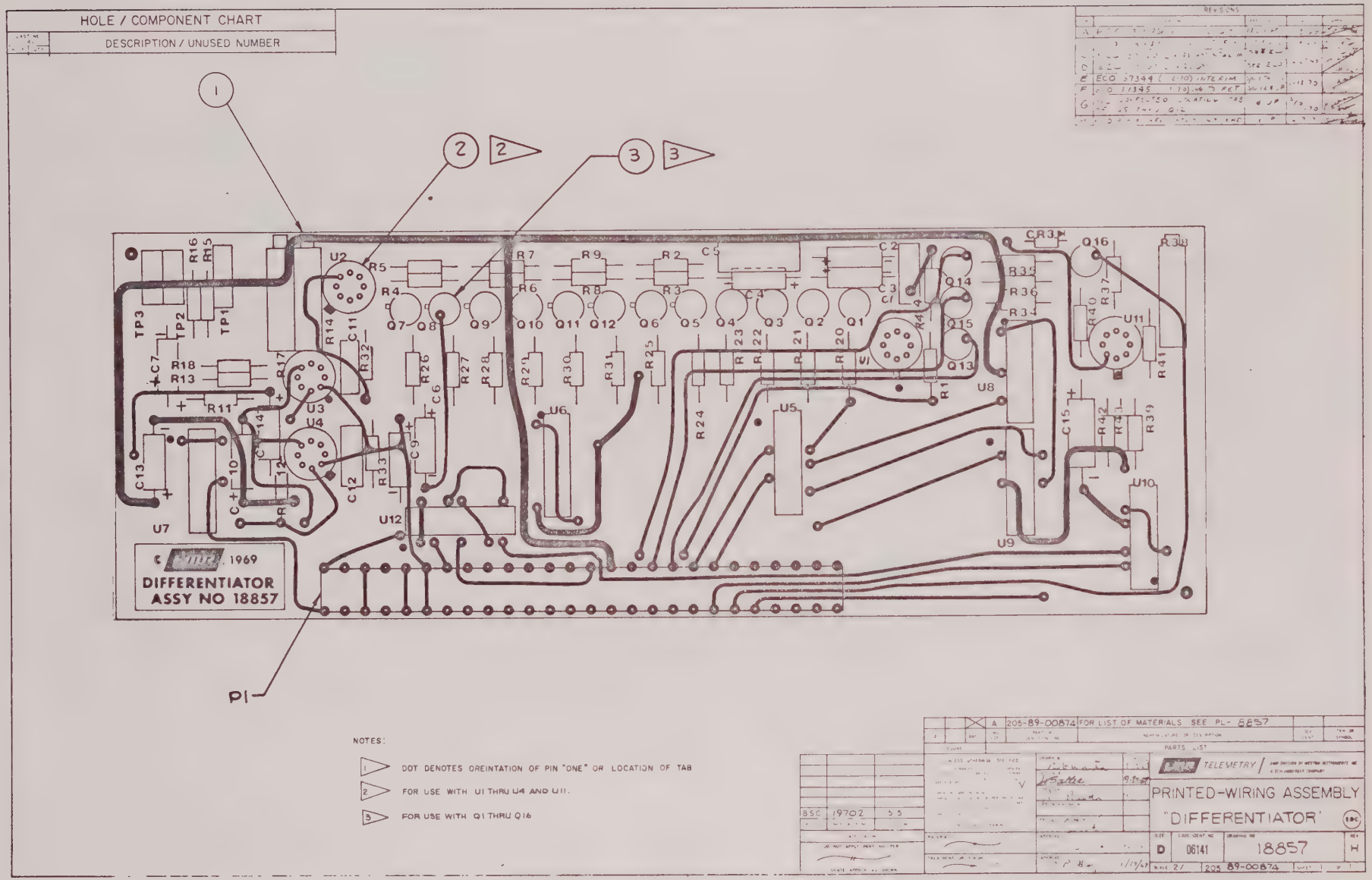


Figure 5-32. Differentiator Printed-Wiring Board Assembly Diagram

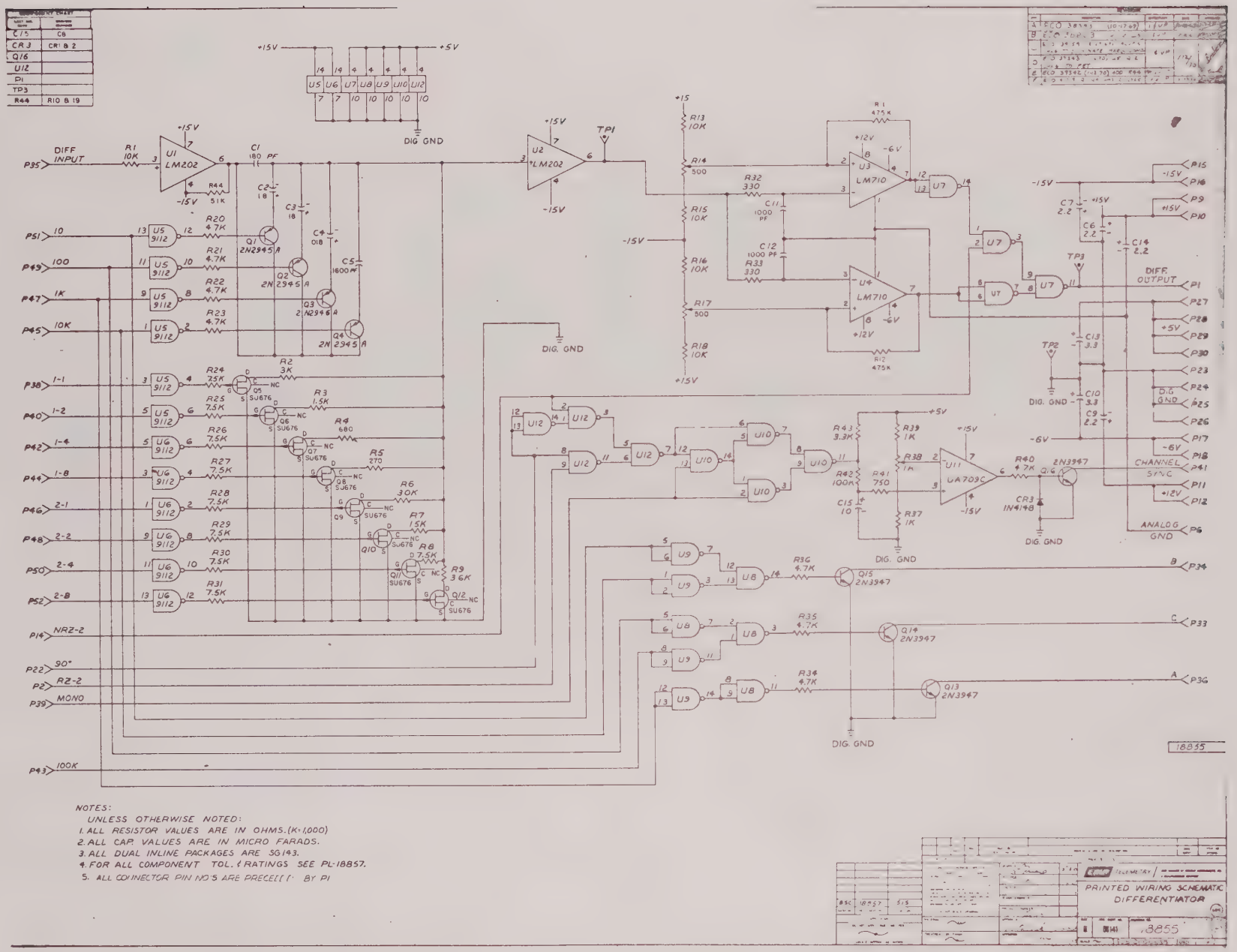


Figure 5-33. Differentiator Printed-Wiring Board Schematic Diagram

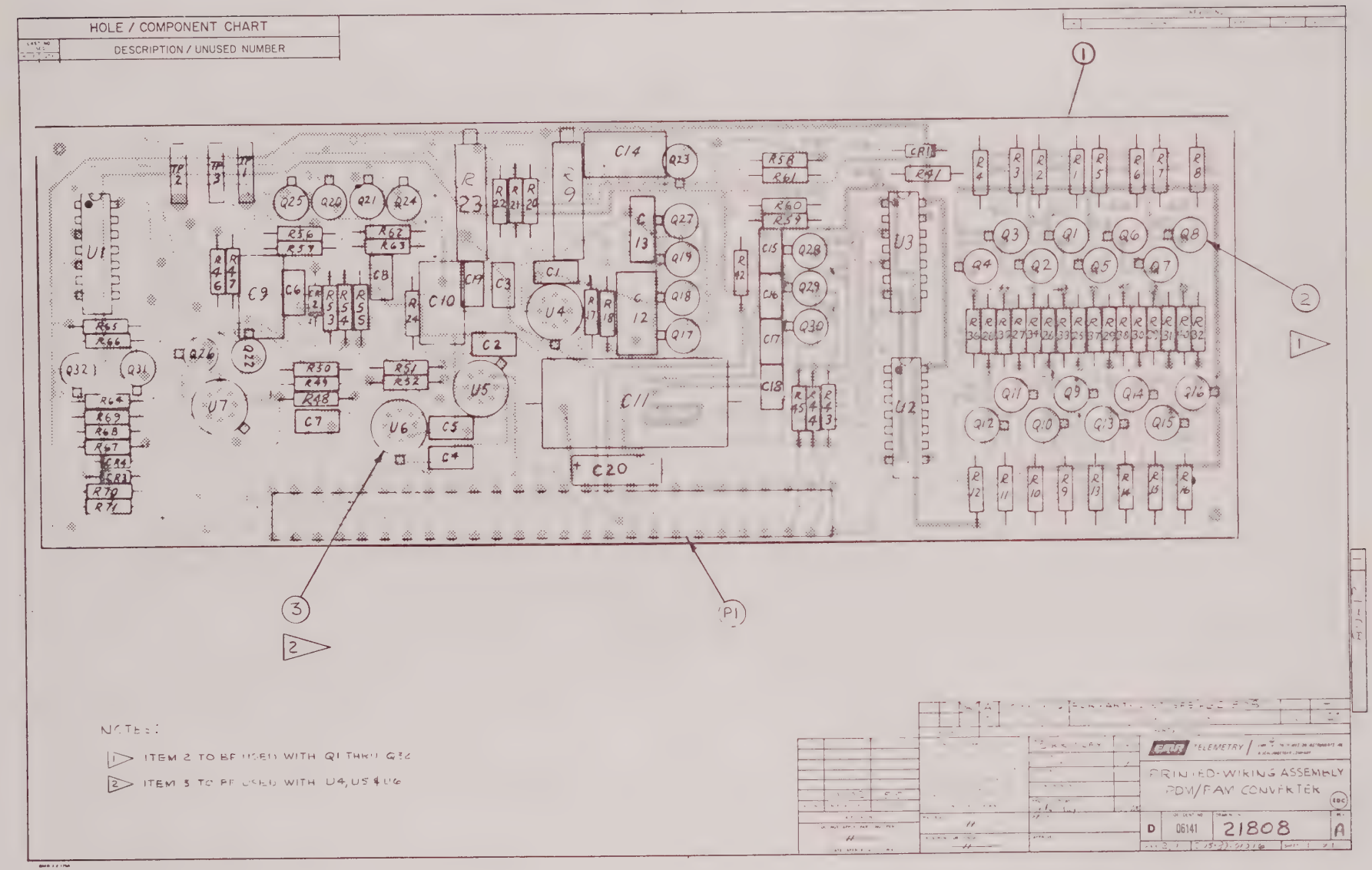


Figure 5-34. PAM/PDM Converter Printed-Wiring Board Assembly Diagram

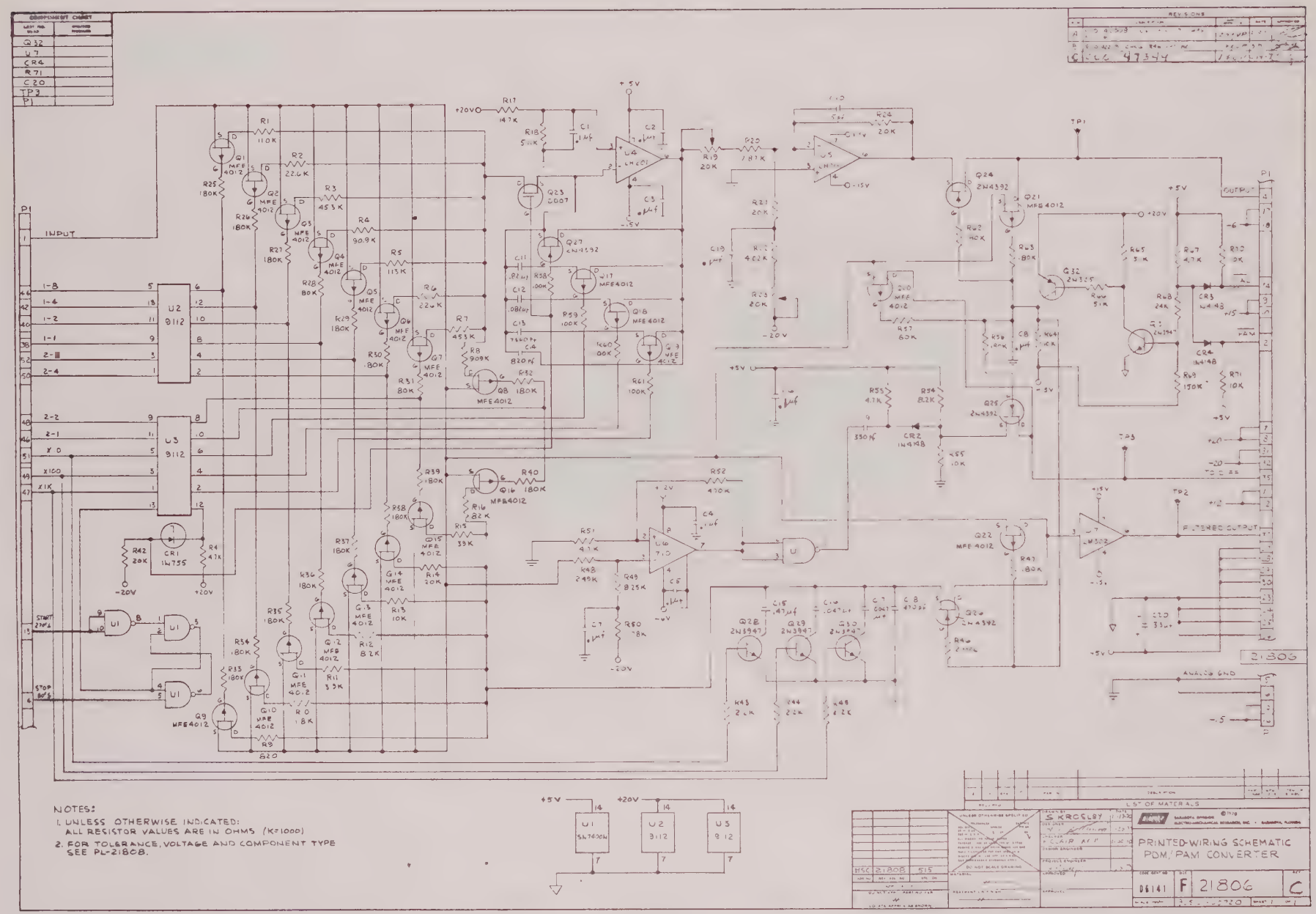


Figure 5-35. PAM/PDM Converter Printed-Wiring Board Schematic Diagram

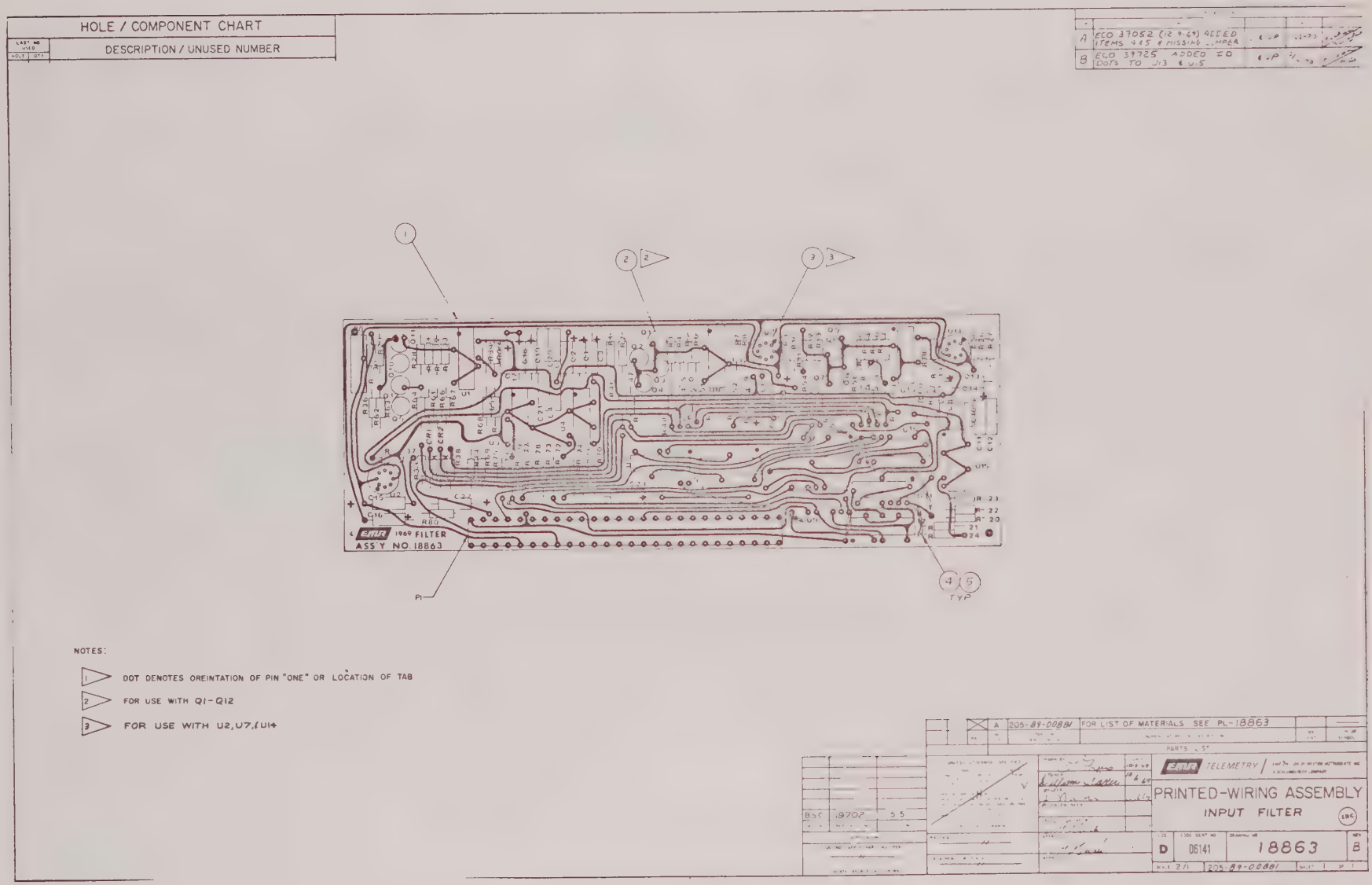


Figure 5-36. Input Filter Printed-Wiring Board Assembly Diagram

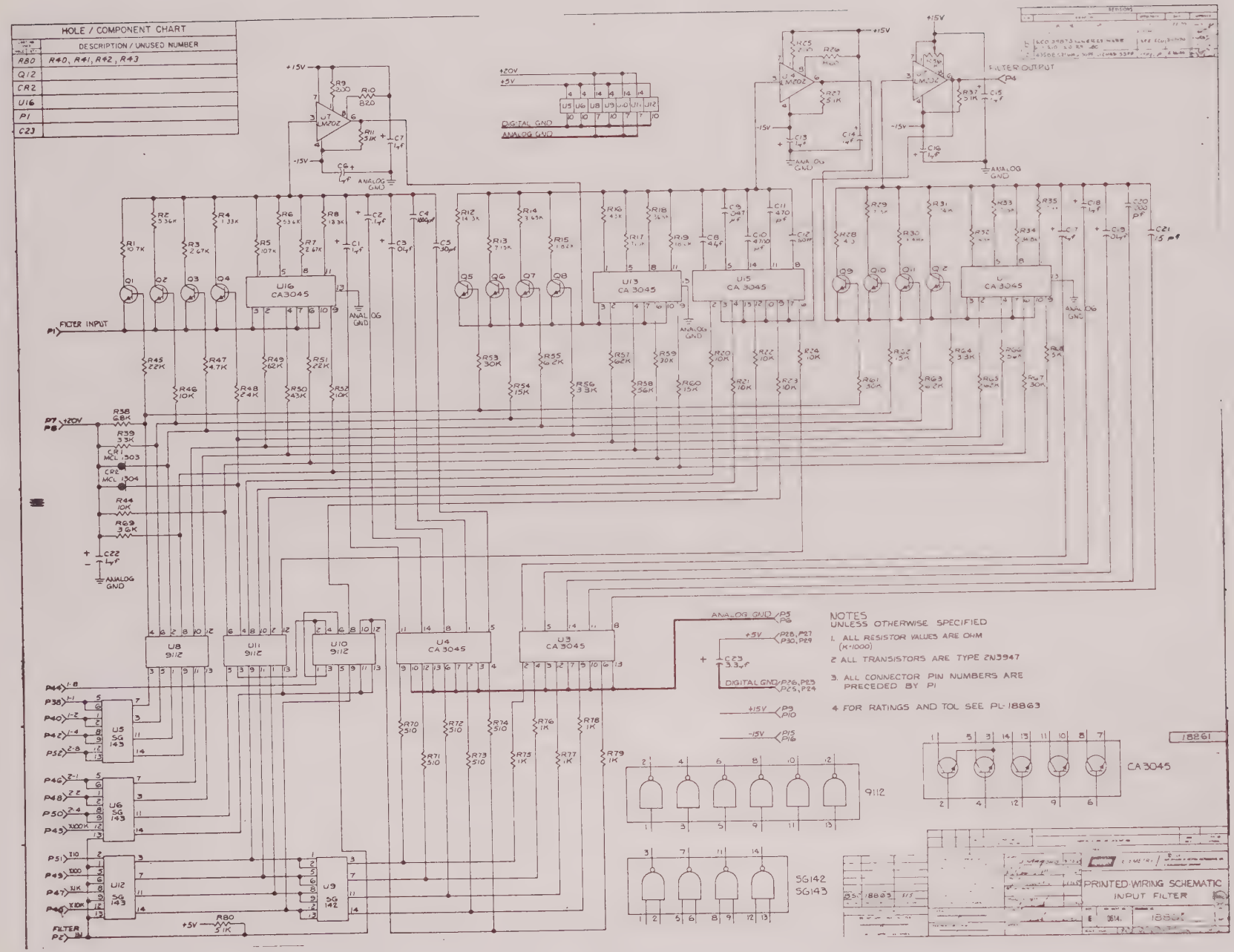


Figure 5-37. Input Filter Printed-Wiring Board Schematic Diagram

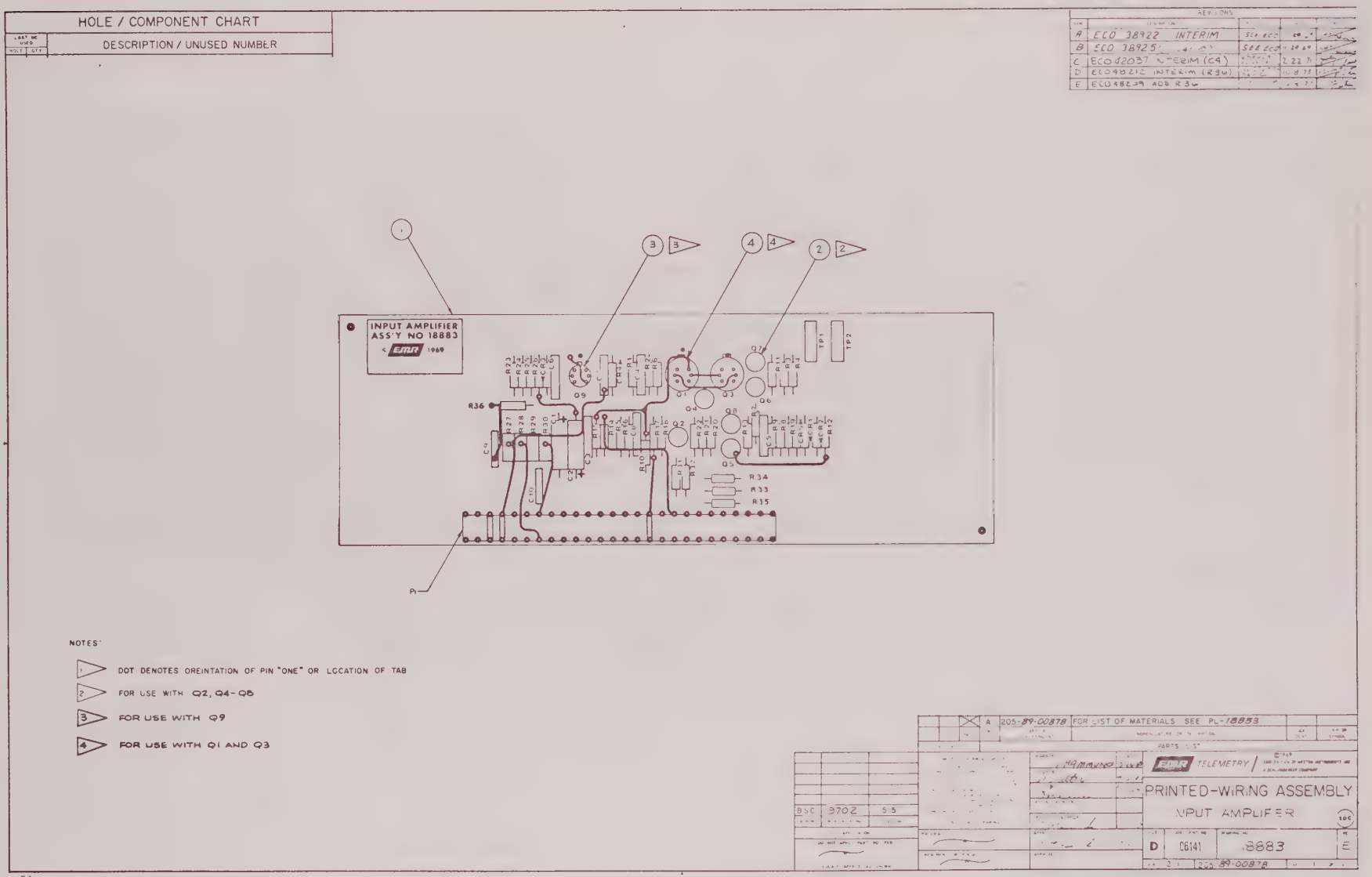
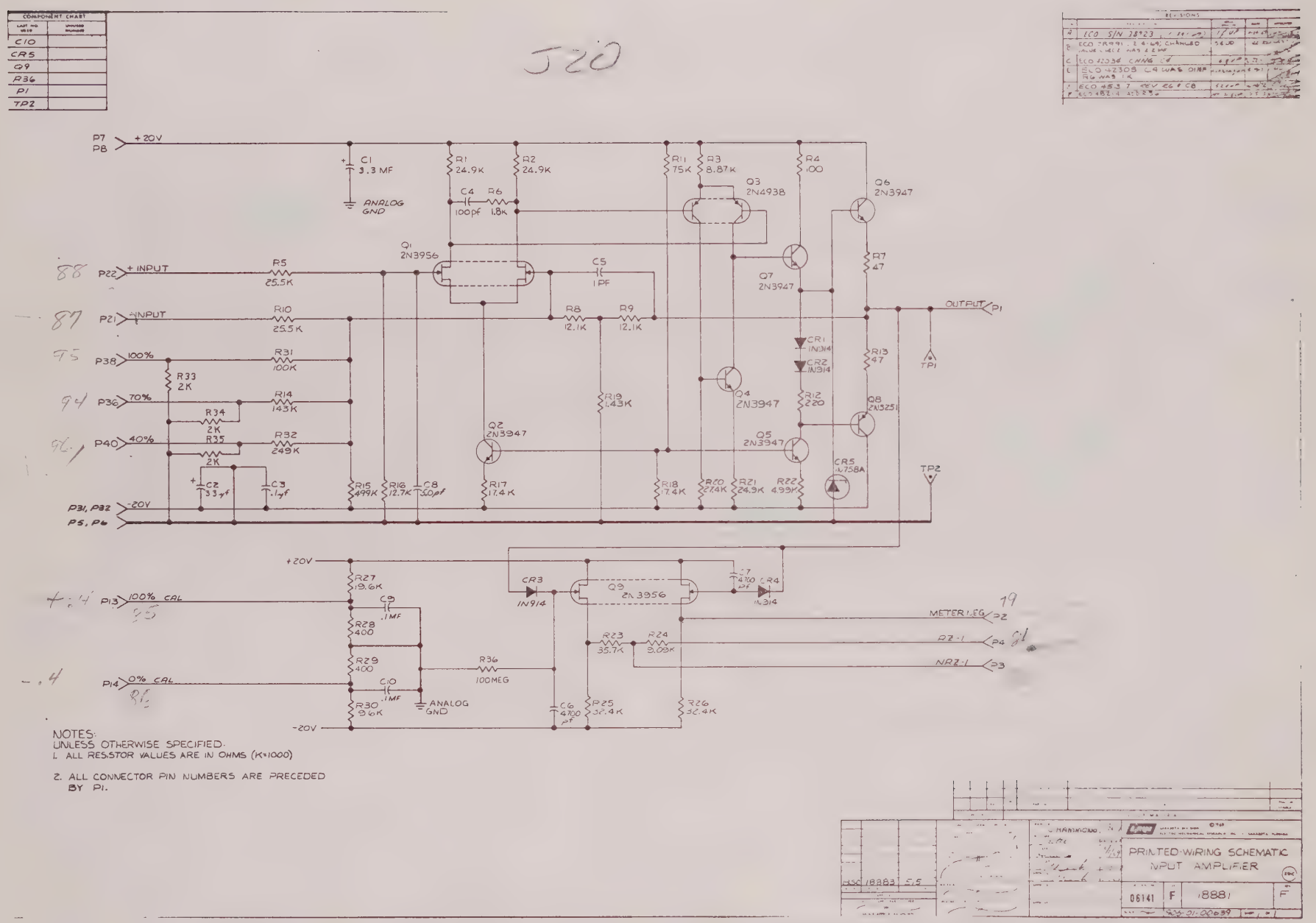


Figure 5-38. Input Amplifier Printed-Wiring Board Assembly Diagram



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTOR VALUES ARE IN OHMS (K=1000)

2. ALL CONNECTOR PIN NUMBERS ARE PRECEDED BY P1.

PRINTED-WIRING SCHEMATIC
INPUT AMPLIFIER

06141 F 18881 F

Figure 5-39. Input Amplifier Printed-Wiring Board Schematic Diagram

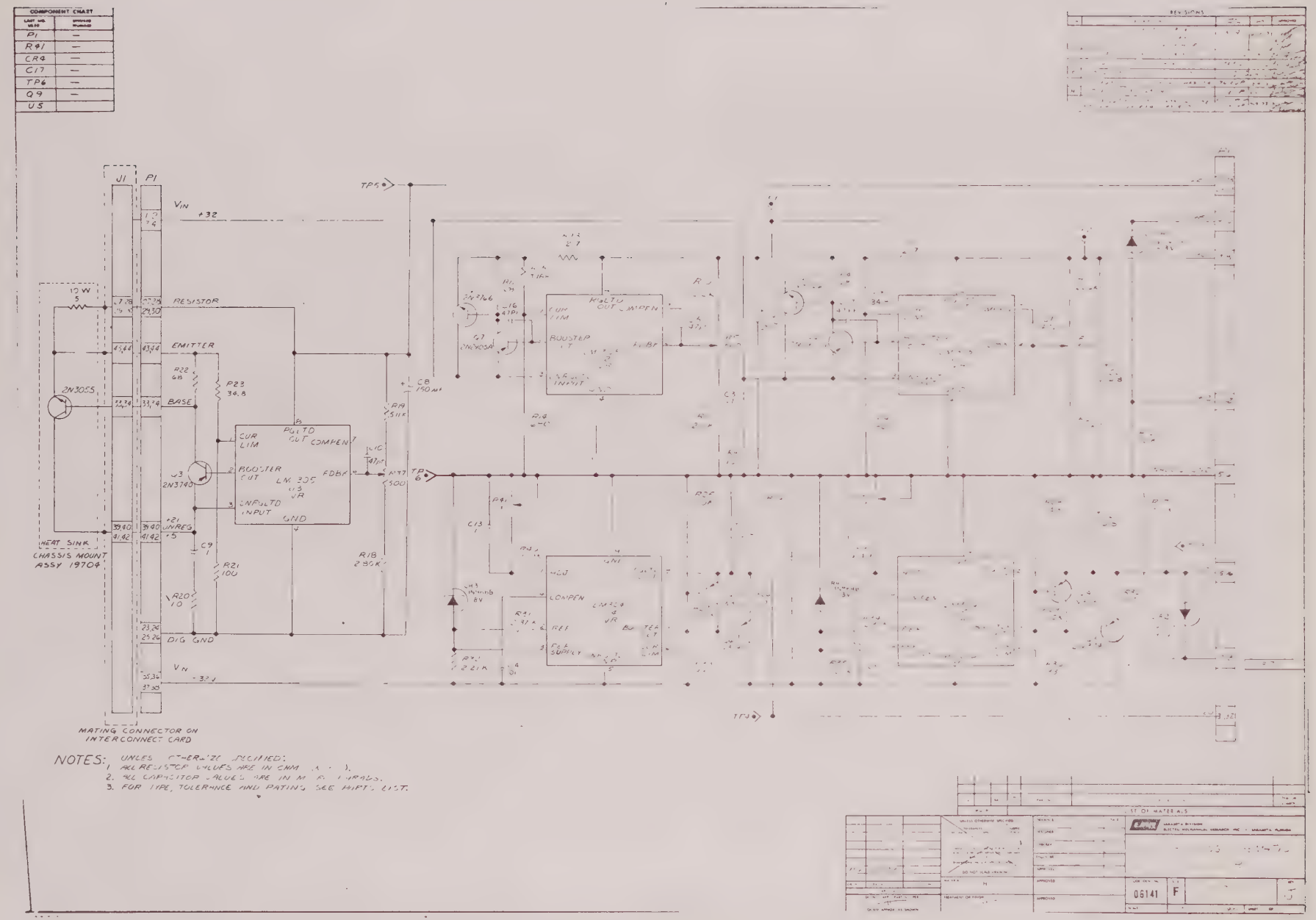


Figure 5-41. Regulator Printed-Wiring Board Schematic Diagram

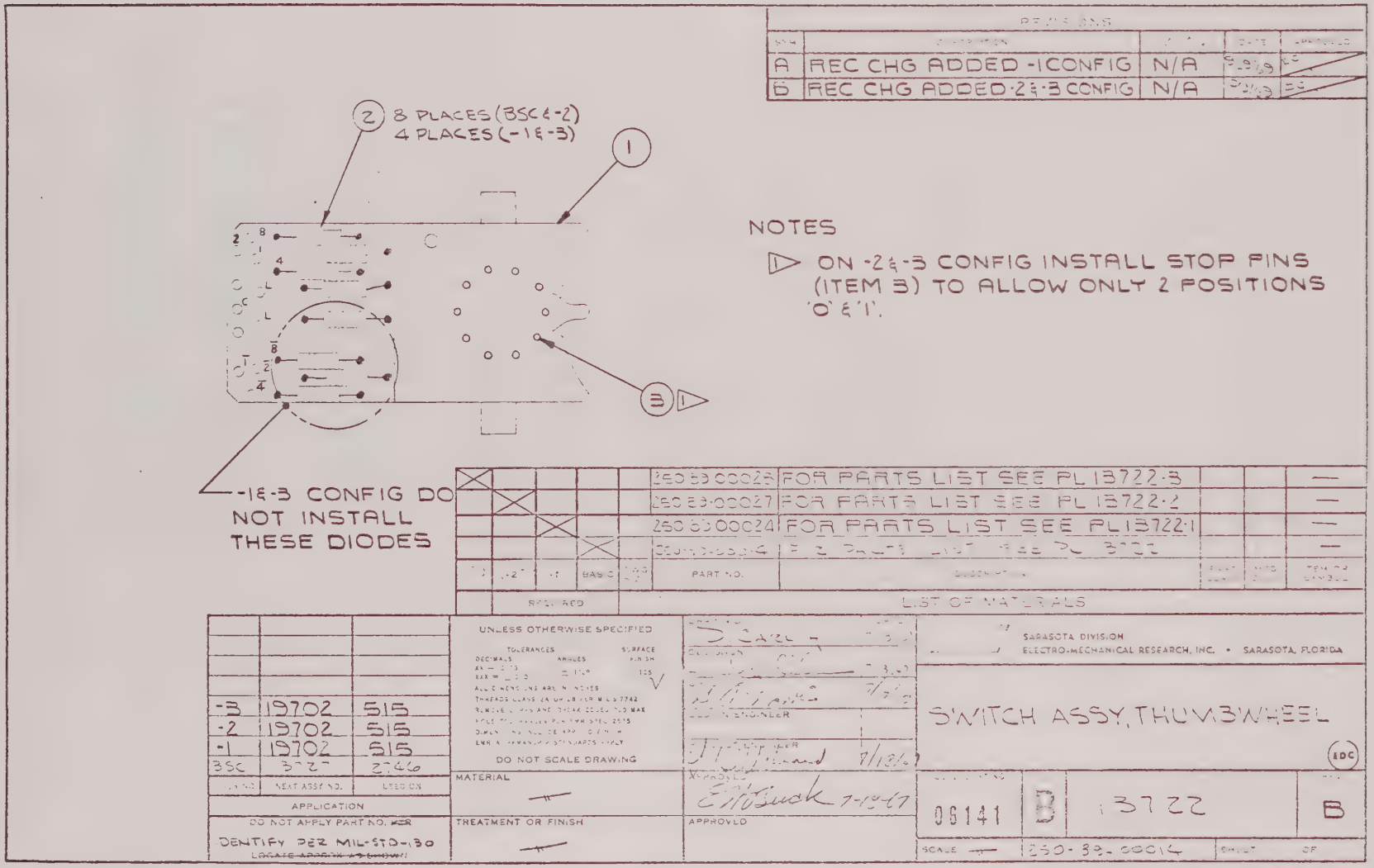
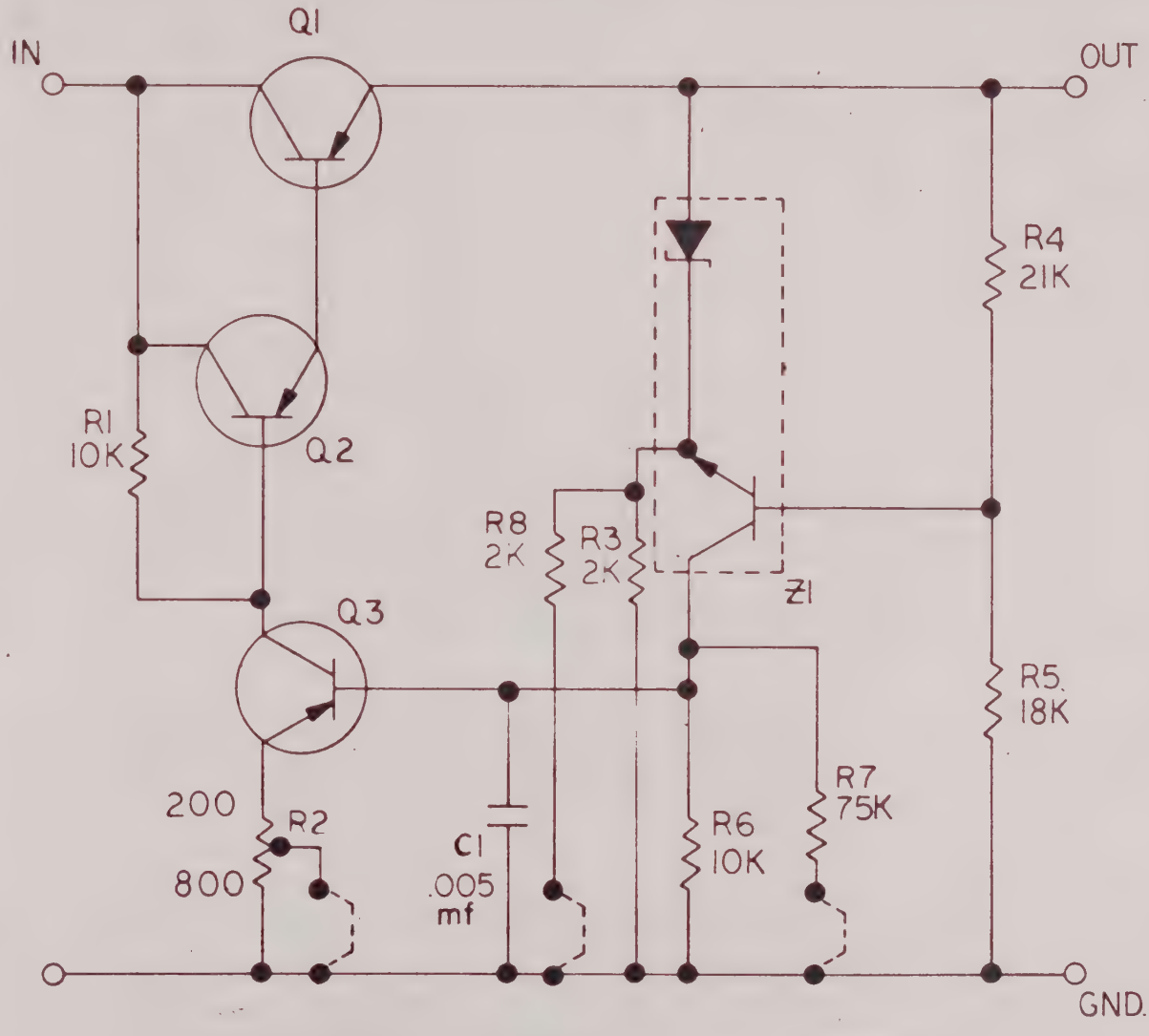


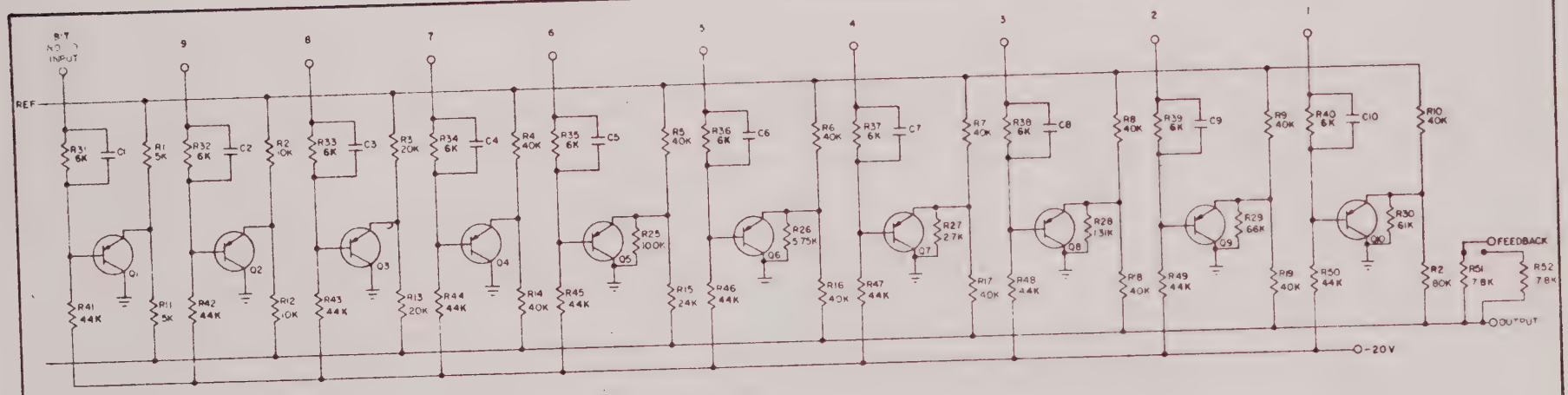
Figure 5-42. Thumbwheel Switch Assembly



NOTES: 1. Q1, Q2, Q3, – 2N2907 IN LID
2. Z1 – DH80112J (EMR 14696)
(DRAL 6.8 B10 IN LID)
3. ALL PINS LOCATED WITHIN .005 TRUE POSITION.
4. ALL RESISTORS ARE DEPOSITED & ETCHED ON SUBSTRATE.

PIN NO.	FUNCTION
1	Input(-20V)
2	Output (-12V)
3	Ground
4	

Figure 5-43. EMR 14817 Integrated Circuit (Reference Regulator)



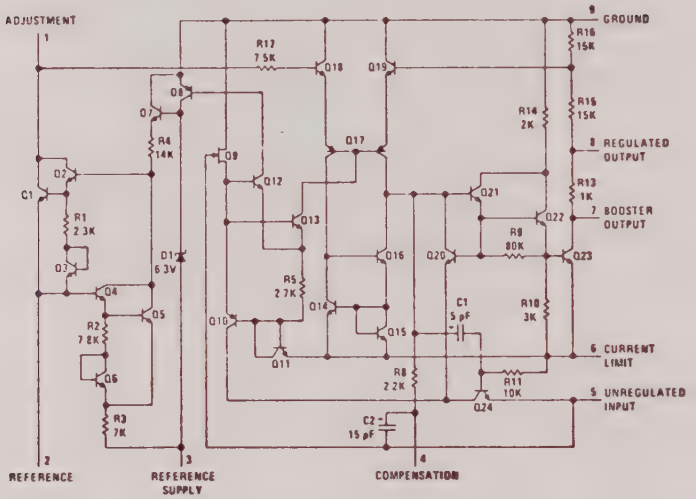
NOTE

1. C1 THRU C10 ARE 470 PF ±20%
2. Q1 THRU Q10 ARE EMR NO 14692
3. ALL RESISTORS ARE DEPOSITED AND ETCHED ON SUBSTRATE.
4. GROUND PINS 5,7 8 9 NOT CONNECTED TO GROUND PINS 12,16 & 20.

PIN #	FUNCTION
1	OUTPUT
2	-20V
3	"BIT 1" IN (LSB)
4	"BIT 2" IN
5	GND
6	"BIT 3" IN
7	GND
8	"BIT 4" IN
9	GND
10	FEEDBACK
11	"BIT 5" IN
12	GND
13	"BIT 6" IN
14	REF. IN
15	"BIT 7" IN
16	GND
17	"BIT 8" IN
18	"BIT 9" IN
19	"BIT 10" IN (MSB)
20	GND

Figure 5-44. EMR 14818 Integrated Circuit (10-Bit Ladder)

schematic and connection diagrams



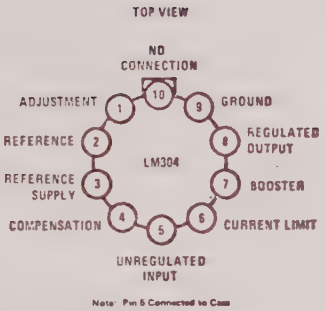


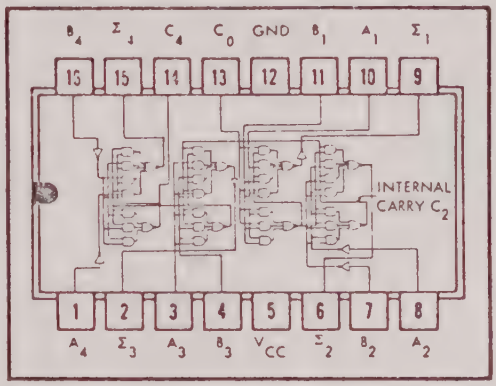
Figure 5-45. National LM304 Integrated Circuit (Negative Regulator)

logic

INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
				WHEN $C_2 = 0$			WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



4-Bit Binary Full Adder

Figure 5-46. Texas Instruments SN7483N Integrated Circuit

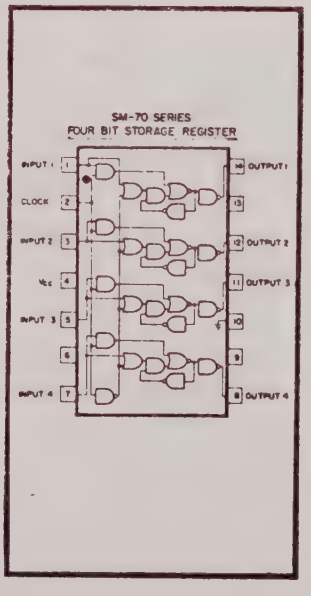
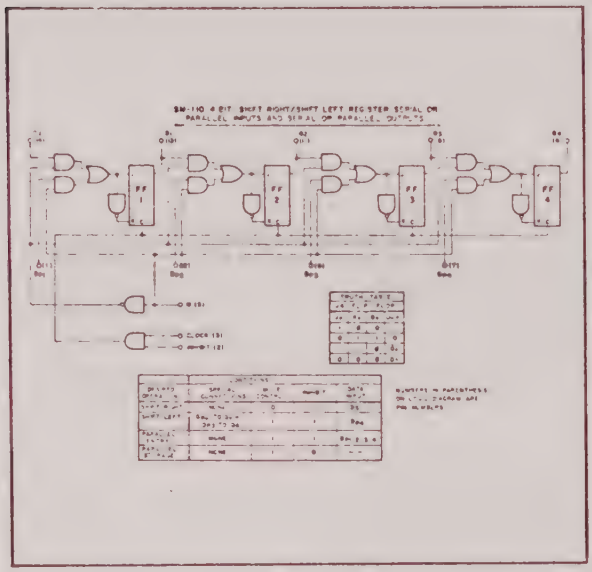
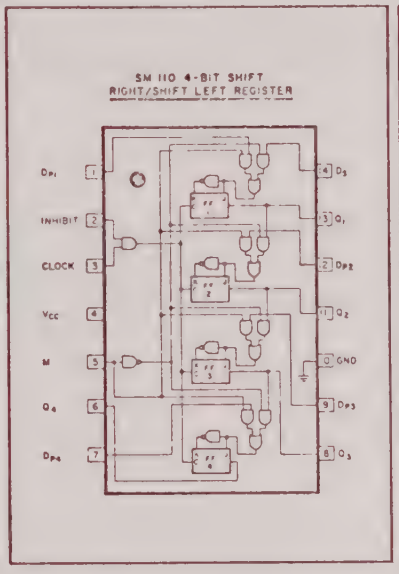


Figure 5-47. Sylvania SM73 Integrated Circuit





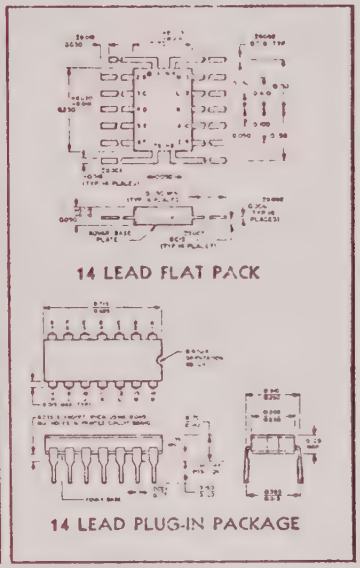
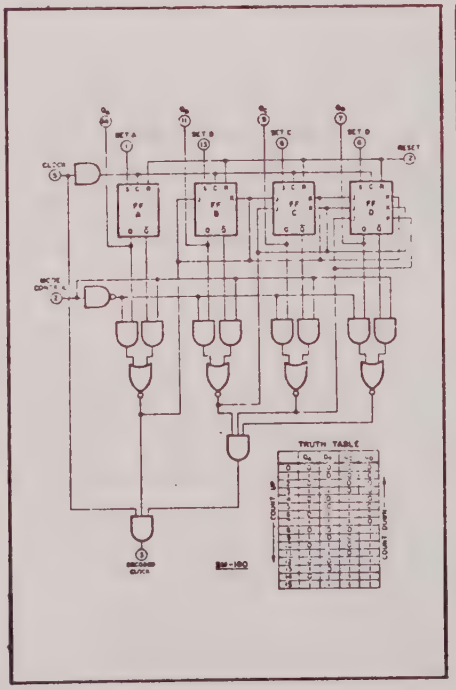
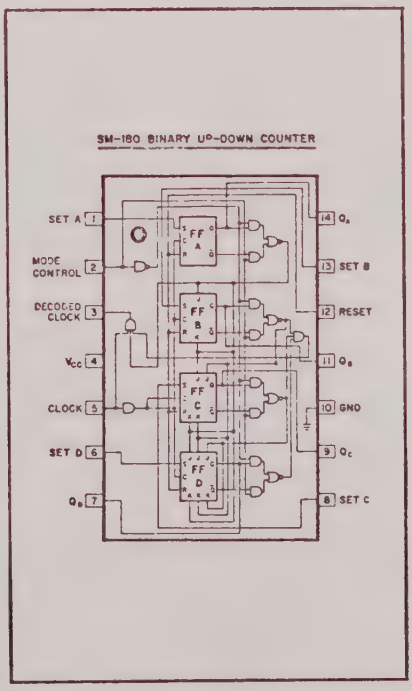


Figure 5-48. Sylvania SM113 Integrated Circuit





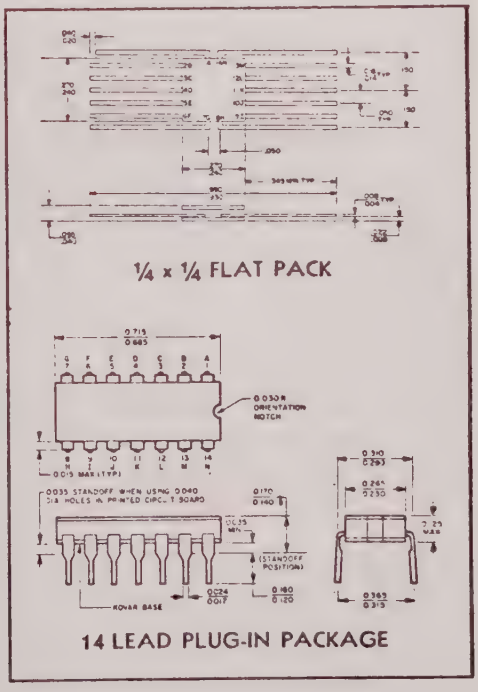


Figure 5-49. Sylvania SM183 Integrated Circuit

SECTION 6

PARTS LISTS AND RECOMMENDED SPARES

6.1 GENERAL

This section contains information concerning parts replacement, spares provisioning, and parts ordering information for the EMR Model 515 PAM/PDM Synchronizer. Paragraph 6.2 describes the parts breakdown for the Model 515 as provided in this manual. Recommended spares, spares provisioning information, and parts ordering instructions are contained in paragraphs 6.3, 6.4, and 6.5, respectively.

6.2 PARTS LIST DESCRIPTION

Table 6-1 identifies the individual parts lists provided in this section for the Model 515 PAM/PDM Synchronizer and references the appropriate assembly diagram for each list. Table 6-2 contains the top-level parts breakdown for the Model 515. This breakdown lists all components mounted directly to the chassis of the Model 515 and its individual subassemblies. Subsequent parts list tables, as identified in Tables 6-1 and 6-2, provide detailed component breakdown of the subassemblies.

The parts list for each assembly contains a listing of all subassemblies and components of the assembly. These subassemblies and/or components are identified by an item number in the ITEM NO. column. The item numbers (or component designation) correspond to numbers in the reference balloons on the associated EMR drawing. Also included in the parts list for each item are the quantity required (QTY REQ'D), EMR PART NUMBER, EMR DRAWING or SPEC. NO. and item DESCRIPTION.

6.3 RECOMMENDED SPARES

A list of the recommended spare parts for the Model 515 is contained in Table 6-27. The recommended spares as listed in this table are based on the following conditions:

a. Operating time -- 8 hours/day, 5 days/week (2080 hours/year).

b. Operating temperature -- 0°C to 50°C.

c. User has capability to repair to the component level.

d. Failure rates are constant.

e. A 0.9 probability of being able to repair from the recommended complement for one year.

f. Equipment will be used as ground equipment (as opposed to vehicular or airborne).

The recommended spares table contains a PART DESCRIPTION column, an EMR STOCK NO. column, a TQ column which is the total quantity of the part in the unit, and an RS column which lists the number of recommended spares for the part.

6.4 PROVISIONING CONSIDERATIONS

The selection of an optimum spare parts complement involves a number of considerations known only to the user. These considerations include operating time and cycles, operating environment, number of equipments to be spared and their locations with respect to one another, urgency of returning an equipment to service, troubleshooting, repair and test capability, stock of commonly used parts, etc.

Sparing considerations known to EMR include mean-time-between-failures for parts and assemblies under various operating environments, prices, relative ease of troubleshooting, repair, retest, etc.

Table 6-28 lists the type of information required in order for EMR to recommend an optimum spare parts complement for specific operating and logistic situations.

If the information outlined in Table 6-28 is supplied to EMR, a recommended list will be furnished at no cost for each individual situation.

6.5 ORDERING INSTRUCTIONS

When ordering parts, EMR stock number and complete description of each part as listed in DESCRIPTION column of parts list must accompany order.

Table 6-1. Parts Lists Identification

ITEM	TABLE NO.	FIGURE NO.
PAM/PDM Synchronizer Assembly	6-2	5-1
Interconnection Board Printed-Wiring Assembly	6-3	5-3
Output Buffer Printed-Wiring Board (Card 2)	6-4	5-4
Decommutator Printed-Wiring Assembly (Card 3)	6-5	5-6
Servo DAC Printed-Wiring Assembly (Card 4)	6-6	5-8
Servo Adder Printed-Wiring Assembly (Card 5)	6-7	5-10
Servo Control Printed-Wiring Assembly (Card 6)	6-8	5-12
A-D Timing Printed-Wiring Assembly (Card 7)	6-9	5-14
Ladder and Switches Printed-Wiring Assembly (Card 8)	6-10	5-16
Sample and Hold Printed-Wiring Assembly (Card 9)	6-11	5-18
Frame Sync Recognition Printed-Wiring Board (Card 10)	6-12	5-20
Channel/Frame Counter Printed-Wiring Assembly (Card 12)	6-13	5-22
Clock Generator Printed-Wiring Assembly (Card 13)	6-14	5-24
VCO Printed-Wiring Assembly (Card 14)	6-15	5-26
Loop Filter Printed-Wiring Assembly (Card 15)	6-16	5-28
Monostable Printed-Wiring Assembly (Card 16)	6-17	5-30
Differentiator Printed-Wiring Assembly (Card 17)	6-18	5-32
PAM/PDM Converter Printed-Wiring Assembly (Card 18)	6-19	5-34
Input Filter Printed-Wiring Assembly (Card 19)	6-20	5-36
Input Amplifier Printed-Wiring Assembly (Card 20)	6-21	5-38
Regulator Printed-Wiring Assembly (Card 21)	6-22	5-40
Thumbwheel Switch Assembly (S8, S9, S11, S12, S14 and S15)	6-23	5-42
Thumbwheel Switch Assembly (S17 and S18)	6-24	5-42
Thumbwheel Switch Assembly (S10, S13, and S16)	6-25	5-42
Thumbwheel Switch Assembly (S19)	6-26	5-42

PARTS LIST 27740-2 REV DATE 11/09/74 REV LTR A

LIST TITLE SYNC,ASSY,PAM/PDM SUBFR CHGE CONT NO. CODE IDENT SHT 1 OF 4

PART NO. 407-89-00024 ECO 50673 06141 CKD BY Brown

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	191-89-00594	27707	PANEL,ASSY,REAR
2	1	282-99-00047	10521	RAIL,SIDE,LEFT
3	1	282-99-00048	10521-1	RAIL,SIDE,RIGHT
4	1	191-99-00365	21903	PANEL FRONT
5	1	298-99-00024	19704	HTSK,TO-3 3LX2.4WX.935H
6	2	128-99-00030	10530	HANDLE
7	1	075-89-00062	10522	COVER,ASSY TCP
8	AR	229-02-00069		SCREW,2-56X1/2 PAN HD
9	AR	229-02-00074		SCREW,4-40X5/16 PAN HD
10	AR	229-02-00239		SCREW,4-40X1-1/4 PAN HD
11	AR	229-02-00257		SCREW,4-40X2 1/4 PAN HD
12	AR	229-02-00084		SCREW,6-32X5/16 PAN HD
13	AR	229-02-00085		SCREW,6-32X3/8 PAN HD
14	AR	229-02-00088		SCREW,6-32X5/8 PAN HD
15	AR	229-02-00101		SCREW,8-32X7/16 PAN HD
16	AR	229-98-00056		SCREW,10-32X1/2,PAN HD
17	AR	273-02-00003		WASHER,#2, FLT ST STL
18	AR	273-02-00005		WASHER,#4, FLT ST STL
19	AR	273-02-00007		WASHER,#6, FLT ST STL
20	AR	273-02-00024		WASHER,#2,INT TOOTH
21	AR	273-02-00025		WASHER,#4,INT TOOTH
22	AR	273-02-00026		WASHER,#6,INT TOOTH
23	AR	273-02-00027		WASHER,#8,INT TOOTH
24	AR	273-02-00028		WASHER,#10,INT TOOTH
25	AR	287-02-00002		NUT,HEX, 4-40
26	2	022-98-00003		BSHG,SHLDR,NYLON,.115ID
27	1	140-98-00006		INS,MICA WASHER TO-3 XSTR
28	AR	060-21-00002		CMPD,HEAT CONDUCTIVE GEL
29	1	016-99-00042	11977	BRKT, SWITCH MOUNTING
30	2	239-99-00094	10525	SPACER,METER
32	1	255-98-00048		TERM,LUG,SOLDER,#4 HOLE
34	2	229-98-00120		SCREW,CAPTIVE PANEL
35	2	415-98-00001		ADPT,1/4 TO 1/8 SHAFT
36	AR	287-02-00003		NUT,HEX, 6-32
37	4	239-98-00026		SPACER,SWITCH ECCO 800
38	3	999-04-00001	19721	KNOB,PCA VAR
39	1	070-98-00016		CORD,W/PLUG,8FT,SJ RUBBER
40	1	063-98-00024		CONN,PLUG,3-WIRE
41	1	126-98-00002		GRILLE,FOR SPRITE FAN
42	AR	999-03-00001	19721	SLIDES,PCA VAR

EDC

Table 6-2 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
43	AR	060-11-00002		CMPD,LOCKING,FINE THREAD
44	6	049-98-00004		CLIP,RETAINER FOR ELDEMA
45	AR	273-98-00022		WASHER,FLAT,FIBER,#6SCREW
46	AR	229-02-00053		SCREW,6-32X1/2 OVAL HEAD
47	1	239-99-00009	6543	SPACER,TEST POINT
48	2	022-98-00002		BSHG,NYLON,BNC CONNECTOR
49	2	273-98-00045		WASHER,PHENOLIC .385 ID
50	2	255-98-00012		TERM,LUG,SOLDER,.375ID
51	2	287-99-00004	10664	NUT,BAR,THUMBWHEEL SW MT
52	AR	229-98-00022		SCREW,SET,4-40X3/32
53	2	239-98-00018		SPACER,#4,.250 OD,.500LG
54	AR	229-02-00080		SCREW,4-40X7/8 PAN HD
55	AR	229-02-00075		SCREW,4-40X3/8 PAN HD
56	AR	229-02-00077		SCREW,4-40X1/2 PAN HD
57	1	063-98-00165		CONN,PLUG, 32 CONTACT R&P
58	1	205-89-00868	18872	PWA, OUTPUT BUFFER
59	1	205-89-00883	18869	PWA,DECOMMUTATOR
60	1	205-89-01594	28090	PWA,SERVO DAC
61	1	205-89-00875	18889	PWA,SERVO ADDER
62	1	205-89-00876	18886	PWA,SERVO CONTROL
63	1	205-89-00870	18839	PWA,TIMING A/D
64	1	205-89-00871	18842	PWA,LADDER & SWITCHES
65	1	205-89-00873	18845	PWA,SAMPLE & HOLD
66	1	205-89-01272	22852	PWA,FRAME SYNC RECOG
67	1	205-89-01029	22066	PWA,CHAN/FRAME COUNTER
68	1	205-89-01028	22063	PWA, CLOCK GENERATOR
69	1	205-89-00877	18854	PWA,VCO
70	1	205-89-00879	18875	PWA,LOOP FILTER
71	1	205-89-00880	18866	PWA,MONOSTABLE
72	1	205-89-00874	18857	PWA,DIFFERENTIATOR
73	1	205-89-00881	18863	PWA,INPUT FILTER
74	1	205-89-00878	18883	PWA,INPUT AMPLIFIER
75	1	205-89-01060	1373	PWA,REGULATOR
76	1	205-89-00885	18880	PWA,INTERCONNECTION
77	1	999-01-00002	19721	PLATE WARNING POA VAR
78	2	229-02-00190		SCREW,4-40X5/8,FLT HD
79	2	239-98-00077		SPACER 1/4DX3/8LX.1401D
80	1	196-99-00154	10526	PLATE,TERM COVER
81	2	287-99-00005	10665	NUT,BAR,THUMBWHEEL SW MT
82	AR	229-98-00056		SCREW,10-32X1/2,PAN HD
85	1	205-89-00889	11073	PWA,EXTENDER CARD
86	2	047-98-00002		CLAMP,CABLE
87	4	284-98-00003		RET,OBSOLETE,USE E-36SG
88	1	196-99-00156	10663	PLATE,NAME EQUIP IDENT

END

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
89	AR	229-02-00087		SCREW,6-32X1/2 PAN HD
90	2	140-99-00117	19717-1	INSUL,CHAS
91	2	140-99-00119	19718	INSUL,CHAS
92	1	140-99-00116	19717	INSUL,CHAS
93	2	284-98-00006		RTNR,PNL SCR,10-32,.187TH
94	AR	999-02-00001	19721	RETRACTOR,POA VAR
95	1	205-89-01016	21808	PWA, PAM/PDM CONVERTER
96	1	246-99-00027	19726	STRIP,IDENT
97	AR	276-98-00081		WIRE,#22,STRD,WHT,600V
98	AR	273-02-00011		WASHER,#10, FLT ST STL
99	AR	229-02-00071		SCREW,2-56X3/4 PAN HD
100	AR	287-02-00001		NUT,HEX, 2-56
101	AR	276-98-00102		WIRE,#24,STRD,WHT,600V
102	AR	276-02-00007		WIRE,#26 STRD,SHLD 2 COND
103	AR	024-02-00001		CABLE, RF COAXIAL
104	1	191-89-00593	27432	PANEL,SUB,SUBASSY
105	1	075-99-00201	27426	COVER,BOTTOM
106	1	075-99-00202	27739	COVER,CONNECTOR
B 1	1	014-98-00006		BLOWER,FAN 115VAC 50/60HZ
DS 1	6	155-98-00016		LIGHT,DISPLAY, RED
THRU				
DS 6				
DS 7	3	155-89-00001	7327	LIGHT,ASSY, DECIMAL
THRU				
DS 9				
DS 10	1	151-02-00001		LAMP,T-1-3/4 28V,.04A
F 1	1	999-01-00001	19721	FUSE,*POA VAR*
J 1	1	063-98-00166		CONN,RECP,32 CONTACT R&P
J 2	1	200-98-00001		POST, BINDING BLACK INSUL
J 3	1	200-98-00003		POST, BINDING, GROUNDED
J 4	1	063-02-00014		CONN,RCPT,BHD,BNC COAX
J 5	1	063-02-00014		CONN,RCPT,BHD,BNC COAX
M 1	1	170-99-00026	16016-6	METER,EDGEWISE,GREEN CTR,
M 2	1	170-99-00027	16016-7	METER,EDGEWISE,ZERO CTR,
M 3	1	170-99-00023	16016-3	METER,EDGEWISE,-100 -5,&1
P 1	1	063-98-00021		CONN,RECP,3-WIRE
Q 1	1	263-10-30550		XSTR,NPN 15A SW-AMPL 100V
R 1	1	638-01-25001	820	RES,VAR,25K 10% 2W
S 1	1	250-98-00157		SW,ROTARY,4SECT 2P,4POSN
S 2	1	250-98-00044		SW,PB,LITED,ALTN,2FORMZ
S 3	1	250-98-00143		SWITCH,ROTARY 2 POLE/4POS
S 4	1	250-98-00088		SW,TOGGLE,DPDT,5A@115VAC
S 5	1	250-98-00025		SW,TOGGLE,SPDT,5A@115VAC
S 6	1	250-98-00025		SW,TOGGLE,SPDT,5A@115VAC

Table 6-2 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
S 7	1	250-98-00088		SW,TOGGLE,DPDT,5A@115VAC
S 8	1	250-89-00014	13722	SWITCH,ASSY,THUMBWHEEL
S 9	1	250-89-00014	13722	SWITCH,ASSY,THUMBWHEEL
S 10	1	250-89-00027	13722-2	SWITCH,ASSY,THUMBWHEEL
S 11	1	250-89-00014	13722	SWITCH,ASSY,THUMBWHEEL
S 12	1	250-89-00014	13722	SWITCH,ASSY,THUMBWHEEL
S 13	1	250-89-00027	13722-2	SWITCH,ASSY,THUMBWHEEL
S 14	1	250-89-00014	13722	SWITCH,ASSY,THUMBWHEEL
S 15	1	250-89-00014	13722	SWITCH,ASSY,THUMBWHEEL
S 16	1	250-89-00027	13722-2	SWITCH,ASSY,THUMBWHEEL
S 17	1	250-89-00024	13722-1	SWITCH,ASSY,THUMBWHEEL
S 18	1	250-89-00024	13722-1	SWITCH,ASSY,THUMBWHEEL
S 19	1	250-89-00028	13722-3	SWITCH,ASSY,THUMBWHEEL
S 20	1	250-98-00144		SW,THUMBWHL,DEC,5POSN,MKD
S 21	3	250-98-00015		SW,THUMBWHL,BCD&CMPLM
THRU S 23				
S 24	5	250-98-00145		SW,THUMBWHL,DEC,4POSN,MKD
THRU S 28				
S 29	1	250-98-00088		SW,TOGGLE,DPDT,5A@115VAC
T 1	1	262-99-00103	18916	XFMR
TP 1	4	143-98-00008		JACK, TEST
THRU TP 4				
XF 1	1	134-98-00006		HLDR,FUSE,3AG,RTANG TERM
A1R 1	1	650-35-00059		RES,.5OHM 1% 10W 50PPM
REF 1	1	999-01-00003	19721	WIRING DIAGRAM,PS,POA VAR
REF 2	1	905-05-00235	19721	VARIABLE CHART 515
REF 3	1	905-14-00196	10645	WIRE LIST,REAR PANEL 515
REF 4	1	905-25-00037	19723	I/O CONN TABLE 515
REF 5	1	905-07-00153	17546	SPEC,ENG,MODEL 515 PAM
REF 6	1	905-14-00226	21902	WIRE LIST,FRONT PANEL AZ

Table 6-3
PARTS LIST 18880 REV DATE 12/10/70 REV LTR B

LIST TITLE PWA,INTERCONNECTION CHGE CONT NO. CODE IDENT SHT 1 OF 2
PART NO. 205-89-00885 ECO 41568 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-89-00339	18879	PWB,INTERCONNECTION
2	A/R	229-98-00070		SCREW,4-40X5/16,PAN HD
3	A/R	060-11-00001		COMP, LOCTITE,GRADE A
4	A/R	273-98-00015		WASHER,#4,FLAT,NYLON
5	20	401-98-00006		GUIDE,CARD
6	4	239-98-00071		SPACER
7	37	239-98-00072		SPACER
8	5	239-98-00073		SPACER
9	2	281-98-00002		STOP
10	2	223-98-00001		ROD
11	1	412-98-00001		IDENT. RET.
13	20	401-98-00007		GUIDE,CARD
14	A/R	276-98-00081		WIRE,#22,STRD,WHT,600V
C 1	1	354-69-22006		CAP., 2200MF,-10, 75%,25
C 2	1	354-65-11006		CAP.,1100 MF -10,&70%,50V

FIRST USAGE MODEL 515

Table 6-3 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
C 3	1	354-65-11006		CAP.,1100 MF -10,&70%,50V
CR 1 THRU CR 3	3	214-98-00017		RECT
R 1	1	616-02-10000		RES,1K 5% 1/4W
R 2	1	616-02-27009		RES,270 OHM 5% 1/4W
REF 1	1	905-13-00118	18878	WIRING DIAGRAM
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

FIRST USAGE MODEL 515

Table 6-4 EMR-TELEMETRY

PARTS LIST 18872 REV DATE 3/22/71 REV LTR A

LIST TITLE PWA, OUTPUT BUFFER CHGE CONT NO. CODE IDENT SHT 1 OF 1
PART NO. 205-89-00868 ECO 42205 06141 CKD BY Braun

ITEM NO.	QTY REQD	EMR NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00575	18871	PWB, OUTPUT BUFFER
C 1	1	336-12-33003	601	CAP., 3.3MF 10% 15V
P 1	1	063-98-00162		CONN, RECP, 52 POSN .150 SP
U 1 thru U 3	3	046-97-00033		INTCKT, QUAD 2IN NAND GATE
REF 1	1	905-01-00629	18870	SCHEMATIC, OUTPUT BUFFER
REF 2	1	905-04-00001	9500	SPEC, COMPONENT SPACING

FIRST USAGE MODEL 515

EMR - TELEMETRY

Table 6-5

PARTS LIST 18869 REV DATE 06/26/72 REV LTR D

LIST TITLE PWA,DECOMMUTATOR CHGE CONT NO. CODE IDENT SHT 1 OF 4
PART NO. 205-89-00883 ECO RECORD 1 C6141 CKD BY Brian

ITEM NO.	QTY REQD	EMR NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00588	18868	PWB,DECOMMUTATOR
2	2	189-99-00005	800-3	PAD,XSTR 8 PIN*USE OPTL*
3	1	298-98-00008		HTSK,FOR TO-5 PKG
4	1	189-99-00001	800-1	PAD,XSTR TO-5,9 OR 11,4 P
5	A/R	276-99-00009	619-24	WIRE,#24,BUSS,SOLID
6	A/R	268-02-00049		TUBING,#24,EXTR TEF,CLEAR
C 1	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 2	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 3	1	304-01-00509	600	CAP. 5PF .5PF 500V
C 4	1	341-06-05609		CAP., 56PF 20% 100V AGED
C 5	1	336-12-33003	601	CAP., 3.3MF 10% 15V
C 6	1	363-39-15000		CAP., 1500PF 10% 100V
C 7	1	304-62-10000	600	CAP. 1000PF 1% 100V
C 8	1	369-34-33000		CAP., 3300PF 10% 200V
C 9	1	304-62-10000	600	CAP. 1000PF 1% 100V

FIRST USAGE MODEL 515

6-10

ECO

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
CR 1	1	088-10-09430		DICDE,REF,11.7V/7.5MA,.00
CR 2	1	088-10-41480		DICDE,SW,75V/5UA,4NS/10MA
CR 3	1	088-10-41480		DICDE,SW,75V/5UA,4NS/10MA
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	1	263-10-37340		XSTR,NPN 1.5A SW-DRIVER
R 1	1	608-09-78709	624	RES, 787.0 OHM 1% 1/10W
R 2	1	608-09-39200	624	RES. 3.92K 1% 1/10W
R 3	1	608-09-22100	624	RES., 2.21K 1% 1/10W
R 4	1	608-09-45300	624	RES, 4.53K 1% 1/10W
R 5	1	616-02-10009		RES,100 OHM 5% 1/4W
R 6	1	201-98-00166		POT.1K 100 PPM CERMET,20
R 7	1	201-98-00160		POT., 200 OHM CERMET PC
R 8	1	201-98-00199		POT., 5K 10% CERMET,2C T
R 9	1	608-09-12101	624	RES, 12.1K 1% 1/10W
R 10	1	608-09-13700	624	RES. 1.37K OHM 1% 1/10W
R 11	1	608-09-10009	624	RES, 100.0 OHM 1% 1/10W
R 12	1	616-02-51009		RES,510 OHM 5% 1/4W

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Table 6-5 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 13	1	616-02-12001		RES,12K 5% 1/4W
R 14	1	616-02-51009		RES,510 OHM 5% 1/4W
R 15	1	616-02-47009		RES,470 OHM 5% 1/4W
R 16	1	616-02-51009		RES,510 OHM 5% 1/4W
R 17	1	616-02-12001		RES,12K 5% 1/4W
R 18	1	616-02-51009		RES,510 OHM 5% 1/4W
R 19	1	616-02-47009		RES,470 OHM 5% 1/4W
R 20	1	608-09-49901	624	RES, 49.9K 1% 1/10W
R 21	1	616-02-51000		RES,5.1K 5% 1/4W
TP 1 THRU TP 3	3	143-98-00037		JACK,TEST BLACK .46 X.23
U 1	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 2 THRU U 4	3	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 6	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 8	1	046-97-00035		INTCKT,*AND* J-K F/F
U 9 THRU U 11	3	046-97-00085		INTCKT,4 BIT STORAGE RGTR

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Table 6-5(Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
U 12	1	046-89-00027	14818	INTCKT,10BIT LADDER
U 13	1	046-89-00026	14817	INTCKT,REF REGULATOR
U 14	1	046-34-00002		INTCKT,OPNL AMPL INT COMP
U 15	1	046-34-00002		INTCKT,OPNL AMPL INT COMP
U 16	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 17	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 18	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
REF 1	1	905-01-00642	18867	SCHEMATIC,PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

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Table 6-8

PARTS LIST 28090 REV DATE 11/09/74 REV LTR A

LIST TITLE PWA,SERVC DAC CHGE CONT NO. CODE IDENT SHT 1 OF 3

PART NO. 205-89-01594 ECO 50667 06141 CKD BY Braun

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-01057	28089	PWB,SERVC DAC
2	1	189-98-00004		PAD,XSTR 4 PIN*USE CPTL*
3	3	189-99-00005	800-3	PAD,XSTR 8 PIN*USE CPTL*
4	AR	268-02-00028		TUBING,#20,EXTR TEF,CLR
C 1	1	301-03-10001		CAP., .01MF 20% 50V LS.10
C 2	1	301-03-10001		CAP., .01MF 20% 50V LS.10
C 3	3	301-13-10002		CAP, .1UF 20% 50V LS.200
THRU C 5				
C 6	1	301-23-22003		CAP., 2.2MF 20% 50V
C 7	1	301-23-22003		CAP., 2.2MF 20% 50V
C 8	1	301-03-10001		CAP., .01MF 20% 50V LS.10
C 9	1	301-03-10001		CAP., .01MF 20% 50V LS.10
C 10	1	301-33-33003		CAP., 3.3MF 20% 50V
C 11	1	301-23-22003		CAP., 2.2MF 20% 50V
C 12	12	301-13-10002		CAP, .1UF 20% 50V LS.200
THRU C 23				
CR 1	1	088-10-09420		DIO,REF,11.7V/7.5MA,.005%
CR 2	1	088-99-00259	642-12	DIODE,1N758A ZENER 10.0V
CR 3	1	088-99-00199	642-06	DIODE,1N752A ZENER 5.6V
CR 4	1	088-10-47441		DIODE,15V/17MA 5% 1W IR
CR 5	1	088-10-47441		DIODE,15V/17MA 5% 1W IR
J 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	1	263-10-39470		XSTR,NPN 40V Sw-AMPL,HFE
Q 2	1	263-10-39470		XSTR,NPN 40V Sw-AMPL,HFE
R 1	1	616-02-68009		RES,68Ω OHM 5% 1/4W
R 2	1	608-09-44200	624	RES. 4.42K 1% 1/10W
R 3	1	608-09-13300	624	RES, 1.33K 1% 1/10W
R 4	1	608-09-26100	624	RES, 2.61K 1% 1/10W
R 5	1	608-09-52300	624	RES. 5.23K 1% 1/10W
R 6	1	608-09-10501	624	RES, 10.5K 1% 1/10W
R 7	1	608-09-10001	624	RES. 10K 1% 1/10W
R 8	1	608-09-00000	624	RES,*TVAR*
R 9	1	608-09-17400	624	RES, 1.74K 1% 1/10W
R 10	1	201-98-00122		POT., 500 OHM 10% .75W PC
R 11	1	201-98-00015		POT., 1K 10% 1W
R 12	1	608-09-49900	624	RES. 4.99K 1% 1/10W
R 13	1	608-09-71500	624	RES. 7.15K 1% 1/10W
R 14	1	608-09-12401	624	RES, 12.4K 1% 1/10W

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 15	1	608-09-69800	624	RES, 6.98K 1% 1/10W
R 16	1	608-09-63400	624	RES, 6.34K 1% 1/10W
R 17	1	616-02-22000		RES,2.2K 5% 1/4W
R 18	1	608-09-22600	624	RES. 2.26K 1% 1/10W
R 19	1	616-02-47009		RES,47C OHM 5% 1/4W
R 20	1	616-02-39000		RES,3.9K 5% 1/4W
R 21	1	616-02-20000		RES,2K 5% 1/4W
R 22	1	616-02-10000		RES,1K 5% 1/4W
R 23	1	616-02-51009		RES,510 OHM 5% 1/4W
R 24	1	616-02-27009		RES,27C OHM 5% 1/4W
R 25	1	616-02-24000		RES,2.4K 5% 1/4W
R 26	1	201-98-00015		POT., 1K 10% 1W
R 27	1	608-09-45300	624	RES, 4.53K 1% 1/10W
R 28	1	608-09-24900	624	RES, 2.49K 1% 1/10W
R 29	1	608-09-00000	624	RES,*TVAR*
R 30	1	608-09-11009	624	RES, 110.0 OHM 1% 1/10W
R 31	1	608-09-11009	624	RES, 110.0 OHM 1% 1/10W
R 32	1	608-01-02009	624	RES, 20.0 OHMS 1% 1/10W 1
R 33	1	626-13-07509	621	RES. 75 OHM 3% 3W
TP 1 THRU TP 3	3	143-98-00051		JACK, TEST, RED
TP 10	1	143-98-00058		JACK, TEST, BLACK
U 1	1	046-34-00002		INTCKT,OPNL AMPL INT COMP
U 2	1	046-34-00002		INTCKT,OPNL AMPL INT COMP
U 3	1	046-97-00151		IC,AMPL,OPNL
U 4	1	046-49-00003		IC,DAC,10BIT BIN,.05% ACC
U 5	1	046-49-00003		IC,DAC,10BIT BIN,.05% ACC
U 6	1	046-97-00050		INTCKT,TRIPLE 3 IN POS
U 7	1	046-97-00044		INTCKT,QUAD,2 INPUT POS
U 8	1	046-97-00044		INTCKT,QUAD,2 INPUT POS
U 9	1	046-97-00111		INTCKT,PROGRAMABLE BINARY
U 10	1	046-97-00056		INTCKT,EXP DUAL 2 WIDE 2
U 11	1	046-97-00056		INTCKT,EXP DUAL 2 WIDE 2
U 12	1	046-97-00065		INTCKT,4 BIT BISTABLE
U 13	1	046-97-00065		INTCKT,4 BIT BISTABLE
U 14	1	046-97-00047		INTCKT,HEX INVERTERS
U 15	1	046-97-00056		INTCKT,EXP DUAL 2 WIDE 2
U 16	1	046-97-00056		INTCKT,EXP DUAL 2 WIDE 2
U 17	1	046-97-00065		INTCKT,4 BIT BISTABLE
U 18	1	046-97-00065		INTCKT,4 BIT BISTABLE
U 19	1	046-97-00044		INTCKT,QUAD,2 INPUT POS
W 1	1	021-98-00005		BUSB,A#.6,B#1.2,C#1.8
W 2	1	021-98-00005		BUSB,A#.6,B#1.2,C#1.8

Table 6-6 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
REF 1	1	905-04-00001	9500	SPEC,COMPONENT SPACING
REF 2	1	905-01-01354	28088	SCHEM,PWA,SERVO DAC

Table 6-7 E M R - T E L E M E T R Y

PARTS LIST 18889 REV DATE 06/26/72 REV LTR A

LIST TITLE PWA,SERVO ADDER CHGE CONT NO. CODE IDENT SHT 1 OF 2
PART NO. 205-89-00875 ECO RECORD 1 06141 CKD BY Brown

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00583	18888	PWB,SERVO ADDER
C 1	1	336-12-33003	601	CAP., 3.3MF 10% 15V
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
U 1	1	046-97-00067		INTCKT,4 BIT BINARY ADDER
U 2	1	046-97-00067		INTCKT,4 BIT BINARY ADDER
U 3	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 4	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 5	1	046-97-00085		INTCKT,4 BIT STORAGE RGTR
U 6	1	046-97-00085		INTCKT,4 BIT STORAGE RGTR
U 7	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 8	1	046-97-00067		INTCKT,4 BIT BINARY ADDER
U 9	1	046-97-00067		INTCKT,4 BIT BINARY ADDER
U 10 THRU U 13	4	046-97-00034		INTCKT,QUAD 2IN NAND GATE
REF 1	1	905-01-00636	18887	SCHEMATIC,PWA

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Table 6-7 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
REF 2	1	905-04-00001	9500	SPEC, COMPONENT SPACING
			FIRST USAGE MODEL 515	

Table 6-8 E M R - T E L E M E T R Y

PARTS LIST 18886 REV DATE 06/26/72 REV LTR B

LIST TITLE PWA,SERVO CONTROL CHGE CONT NO. CODE IDENT SHT 1 OF 2
PART NO. 205-89-00876 ECO RECORD 1 06141 CKD BY Brain.

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00584	18885	PWB,SERVO CONTROL
2	4	189-98-00004		PAC,XSTR 4 PIN*USE OPTL*
C 1	1	336-12-33003	601	CAP.,3.3MF 10% 15V
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1 THRU Q 4	4	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
R 1	1	616-02-27009		RES,270 OHM 5% 1/4W
R 2 THRU R 5	4	616-02-47000		RES,4.7K 5% 1/4W
R 6 THRU R 10	7	616-02-22000		RES,2.2K 5% 1/4W
U 1	1	046-97-00067		INTCKT,4 BIT BINARY ADDER
U 2	1	046-97-00085		INTCKT,4 BIT STORAGE RGTR
U 3	1	046-97-00067		INTCKT,4 BIT BINARY ADDER
U 4 THRU U 7	4	046-97-00034		INTCKT,QUAD 2IN NAND GATE

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Table 6-8 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
U 8	1	046-97-00085		INTCKT,4 BIT STORAGE RGTR
U 9	1	046-97-00085		INTCKT,4 BIT STORAGE RGTR
U 10	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 11	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 12	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 13	1	046-97-00029		INTCKT,DUAL 4IN NAND GATE
U 14	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 15	1	046-97-00039		INTCKT,*OR* J-K F/F FAN 6
U 16	1	046-97-00039		INTCKT,*OR* J-K F/F FAN 6
U 17	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 18	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
REF 1	1	905-04-00001	9500	SPEC,COMPONENT SPACING
REF 2	1	905-01-00637	18884	SCHEMATIC,PWA

FIRST USAGE MODEL 515

Table 6-9

PARTS LIST 18839 REV DATE 12/05/74 REV LTR F

LIST TITLE PWA,TIMING A/D CHGE CONT NO. CODE IDENT SHT 1 OF 2

PART NO. 205-89-00870 ECO 50687 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00577	18838	PWB,TIMING A/D
2	5	189-98-00004		PAD,XSTR 4 PIN*USE OPTL*
C 1	1	304-13-05009	600	CAP. 5OPF 1% 500V
C 2	1	336-12-33003	601	CAP., 3.3MF 10% 15V
C 3	1	336-12-33003	601	CAP., 3.3MF 10% 15V
C 4	1	304-08-03609	600	CAP. 36PF .5PF 500V
C 5	1	304-08-03609	600	CAP. 36PF .5PF 500V
C 6	1	304-20-10009	600	CAP. 100PF 1% 500V
C 7	1	336-12-33003	601	CAP., 3.3MF 10% 15V
CR 3	1	088-99-00339	642-03	DIODE,1N749A ZENER 4.3V
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1 THRU Q 5	5	263-10-08340		XSTR,NPN 350MHZ SW,ON 35N
R 1	1	616-02-47009		RES,470 OHM 5% 1/4W
R 2	1	616-02-51009		RES,510 OHM 5% 1/4W
R 3	1	616-02-01509		RES,15 OHM 5% 1/4W
R 4	1	616-02-56009		RES,560 OHM 5% 1/4W
R 5	1	616-02-10001		RES,10K 5% 1/4W
R 6	1	616-02-56009		RES,560 OHM 5% 1/4W
R 7	1	608-09-90900	624	RES. 9.09K 1% 1/10W
R 8	1	608-09-90900	624	RES. 9.09K 1% 1/10W
R 9	1	616-02-56009		RES,560 OHM 5% 1/4W
R 10	1	616-02-10001		RES,10K 5% 1/4W
R 11	1	616-02-56009		RES,560 OHM 5% 1/4W
R 12	1	616-02-18001		RES,18K 5% 1/4W
R 13	1	616-02-30001		RES,30K 5% 1/4W
R 14	1	616-02-39000		RES,3.9K 5% 1/4W
R 15	1	608-09-51109	624	RES, 511.0 OHM 1% 1/10W
U 1	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 2	1	046-97-00035		INTCKT,*AND* J-K F/F
U 3	1	046-97-00072		INTCKT,4 BIT RIGHT SHIFT
U 4 THRU U 7	4	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 8	1	046-97-00085		INTCKT,4 BIT STORAGE RGTR
U 9	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 10	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 11	1	046-97-00072		INTCKT,4 BIT RIGHT SHIFT
U 12 THRU	4	046-97-00034		INTCKT,QUAD 2IN NAND GATE

Table 6-9 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
U 16	1	046-97-00085		INTCKT,4 BIT STORAGE RGTR
U 17	1	046-97-00072		INTCKT,4 BIT RIGHT SHIFT
U 18	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 19 THRU U 21	3	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 22	1	046-97-00085		INTCKT,4 BIT STORAGE RGTR
REF 1	1	905-01-00631	18837	SCHEMATIC,PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

Table 6-10

PARTS LIST 18842 REV DATE 03/14/74 REV LTR M

LIST TITLE PWA,LADDER & SWITCHES CHGE CONT NO. CODE IDENT SHT 1 OF 5

PART NO. 205-89-00871 ECO RECORD 1 06141 CKD BY Brown.

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00579	18841	PWB,LADDER & SWITCHES
2	1	189-98-00016		PAD,XSTR,TO-5 8PIN,.075H
3	40	189-98-00024		PAD,XSTR TO-18 4 PIN,.022
4	AR	276-02-00007		WIRE,#26 STRD,SHLD 2 COND
C 1	1	363-34-47009		CAP., 470PF 10% 200V
C 2	1	363-34-56008		CAP., 56PF 10% 200V
C 3	3	363-34-47009		CAP., 470PF 10% 200V
THRU C 5				
C 6	1	363-34-56008		CAP., 56PF 10% 200V
C 7	3	363-34-47009		CAP., 470PF 10% 200V
THRU C 9				
C 10	1	363-34-56008		CAP., 56PF 10% 200V
C 11	3	363-34-47009		CAP., 470PF 10% 200V
THRU C 13				
C 14	1	363-34-56008		CAP., 56PF 10% 200V
C 15	3	363-34-47009		CAP., 470PF 10% 200V
THRU C 17				
C 18	1	363-34-56008		CAP., 56PF 10% 200V
C 19	3	363-34-47009		CAP., 470PF 10% 200V
THRU C 21				
C 22	1	363-34-56008		CAP., 56PF 10% 200V
C 23	3	363-34-47009		CAP., 470PF 10% 200V
THRU C 25				
C 26	1	363-34-56008		CAP., 56PF 10% 200V
C 27	3	363-34-47009		CAP., 470PF 10% 200V
THRU C 29				
C 30	1	363-34-56008		CAP., 56PF 10% 200V
C 31	3	363-34-47009		CAP., 470PF 10% 200V
THRU C 33				
C 34	1	363-34-56008		CAP., 56PF 10% 200V
C 35	3	363-34-47009		CAP., 470PF 10% 200V
THRU				

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
C 38	1	363-34-56008		CAP., 56PF 10% 200V
C 39	1	363-34-47009		CAP., 470PF 10% 200V
C 40	1	363-34-47009		CAP., 470PF 10% 200V
C 41	3	336-13-22003	601	CAP. 2.2MF 10% 20V
THRU				
C 43				
C 44	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 45	1	337-14-68003	601	CAP. 6.8MF 10% 35V
C 46	1	305-20-10000	600	CAP., 1000PF 1% NON-STD
C 47	1	336-13-22003	601	CAP. 2.2MF 10% 20V
CR 1	10	088-99-00259	642-12	DIODE,1N758A ZENER 10.0V.
THRU				
CR 10				
CR 11	1	088-10-47431		DIODE,13V/19MA 5% 1W TR
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 2	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 3	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 4	1	263-10-24320		XSTR
Q 5	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 6	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 7	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 8	1	263-10-24320		XSTR
Q 9	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 10	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 11	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 12	1	263-10-24320		XSTR
Q 13	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 14	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 15	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 16	1	263-10-24320		XSTR
Q 17	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 18	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 19	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 20	1	263-10-24320		XSTR
Q 21	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 22	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 23	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 24	1	263-10-24320		XSTR
Q 25	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 26	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 27	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 28	1	263-10-24320		XSTR
Q 29	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V

Table 6-10 (Cont'd.).

ITEM NO.	QTY REQD	F M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
Q 30	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 31	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 32	1	263-10-24320		XSTR
Q 33	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 34	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 35	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 36	1	263-10-24320		XSTR
Q 37	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 38	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 39	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 40	1	263-10-24320		XSTR
R 1	1	616-02-20001		RES,20K 5% 1/4W
R 2	1	616-02-20001		RES,20K 5% 1/4W
R 3	1	616-02-68000		RES,6.8K 5% 1/4W
R 4	1	616-02-27000		RES,2.7K 5% 1/4W
R 5	1	616-02-27000		RES,2.7K 5% 1/4W
R 6	1	616-02-43000		RES,4.3K 5% 1/4W
R 7	1	616-02-30001		RES,30K 5% 1/4W
R 8	1	616-02-30001		RES,30K 5% 1/4W
R 9	1	616-02-20001		RES,20K 5% 1/4W
R 10	1	616-02-20001		RES,20K 5% 1/4W
R 11	1	616-02-68000		RES,6.8K 5% 1/4W
R 12	1	616-02-27000		RES,2.7K 5% 1/4W
R 13	1	616-02-27000		RES,2.7K 5% 1/4W
R 14	1	616-02-43000		RES,4.3K 5% 1/4W
R 15	1	616-02-30001		RES,30K 5% 1/4W
R 16	1	616-02-30001		RES,30K 5% 1/4W
R 17	1	616-02-20001		RES,20K 5% 1/4W
R 18	1	616-02-20001		RES,20K 5% 1/4W
R 19	1	616-02-68000		RES,6.8K 5% 1/4W
R 20	1	616-02-27000		RES,2.7K 5% 1/4W
R 21	1	616-02-27000		RES,2.7K 5% 1/4W
R 22	1	616-02-43000		RES,4.3K 5% 1/4W
R 23	1	616-02-30001		RES,30K 5% 1/4W
R 24	1	616-02-30001		RES,30K 5% 1/4W
R 25	1	616-02-20001		RES,20K 5% 1/4W
R 26	1	616-02-20001		RES,20K 5% 1/4W
R 27	1	616-02-68000		RES,6.8K 5% 1/4W
R 28	1	616-02-27000		RES,2.7K 5% 1/4W
R 29	1	616-02-27000		RES,2.7K 5% 1/4W
R 30	1	616-02-43000		RES,4.3K 5% 1/4W
R 31	1	616-02-30001		RES,30K 5% 1/4W
R 32	1	616-02-30001		RES,30K 5% 1/4W
R 33	1	616-02-20001		RES,20K 5% 1/4W

Table 6-10 (Cont d.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 34	1	616-02-20001		RES,20K 5% 1/4W
R 35	1	616-02-68000		RES,6.8K 5% 1/4W
R 36	1	616-02-27000		RES,2.7K 5% 1/4W
R 37	1	616-02-27000		RES,2.7K 5% 1/4W
R 38	1	616-02-43000		RES,4.3K 5% 1/4W
R 39	1	616-02-30001		RES,30K 5% 1/4W
R 40	1	616-02-30001		RES,30K 5% 1/4W
R 41	1	616-02-20001		RES,20K 5% 1/4W
R 42	1	616-02-20001		RES,20K 5% 1/4W
R 43	1	616-02-68000		RES,6.8K 5% 1/4W
R 44	1	616-02-27000		RES,2.7K 5% 1/4W
R 45	1	616-02-27000		RES,2.7K 5% 1/4W
R 46	1	616-02-43000		RES,4.3K 5% 1/4W
R 47	1	616-02-30001		RES,30K 5% 1/4W
R 48	1	616-02-30001		RES,30K 5% 1/4W
R 49	1	616-02-20001		RES,20K 5% 1/4W
R 50	1	616-02-20001		RES,20K 5% 1/4W
R 51	1	616-02-68000		RES,6.8K 5% 1/4W
R 52	1	616-02-27000		RES,2.7K 5% 1/4W
R 53	1	616-02-27000		RES,2.7K 5% 1/4W
R 54	1	616-02-43000		RES,4.3K 5% 1/4W
R 55	1	616-02-30001		RES,30K 5% 1/4W
R 56	1	616-02-30001		RES,30K 5% 1/4W
R 57	1	616-02-20001		RES,20K 5% 1/4W
R 58	1	616-02-20001		RES,20K 5% 1/4W
R 59	1	616-02-68000		RES,6.8K 5% 1/4W
R 60	1	616-02-27000		RES,2.7K 5% 1/4W
R 61	1	616-02-27000		RES,2.7K 5% 1/4W
R 62	1	616-02-43000		RES,4.3K 5% 1/4W
R 63	1	616-02-30001		RES,30K 5% 1/4W
R 64	1	616-02-30001		RES,30K 5% 1/4W
R 65	1	616-02-20001		RES,20K 5% 1/4W
R 66	1	616-02-20001		RES,20K 5% 1/4W
R 67	1	616-02-68000		RES,6.8K 5% 1/4W
R 68	1	616-02-27000		RES,2.7K 5% 1/4W
R 69	1	616-02-27000		RES,2.7K 5% 1/4W
R 70	1	616-02-43000		RES,4.3K 5% 1/4W
R 71	1	616-02-30001		RES,30K 5% 1/4W
R 72	1	616-02-30001		RES,30K 5% 1/4W
R 73	1	616-02-20001		RES,20K 5% 1/4W
R 74	1	616-02-20001		RES,20K 5% 1/4W
R 75	1	616-02-68000		RES,6.8K 5% 1/4W
R 76	1	616-02-27000		RES,2.7K 5% 1/4W
R 77	1	616-02-27000		RES,2.7K 5% 1/4W

Table 6-10 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 78	1	616-02-43000		RES,4.3K 5% 1/4W
R 79	1	616-02-30001		RES,30K 5% 1/4W
R 80	1	616-02-30001		RES,30K 5% 1/4W
R 81	1	622-02-15009		RES, 150 OHM 5% 1/2W
U 1	1	182-99-00004	932-2	NET.,RESISTOR LADDER
U 2	1	046-34-00013		INTCKT, VOLTAGE COMPTR
REF 1	1	905-01-00632	18840	SCHEMATIC,PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

Table 6-11

PARTS LIST 19845 REV DATE 03/14/74 REV LTR B

LIST TITLE PWA,SAMPLE & HOLD CHGE CONT NO. CODE IDENT SHT 1 OF 2

PART NO. 205-89-00873 ECO RECORD 1 06141 CKD BY Brown

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00581	18844	PWB,SAMPLE & HOLD
2	2	189-98-00005		PAD,XSTR TO-5,9 CR 11,6 P
3	15	189-98-00004		PAD,XSTR 4 PIN*USE CPTL*
4	2	189-98-00030		PAD,XSTR TO-18 8 PIN
C 1	1	304-20-10009	600	CAP. 100PF 1% 500V
C 2	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 3	1	304-62-10000	600	CAP. 1000PF 1% 100V
C 4	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 5	1	304-01-01509	600	CAP. 15PF .5PF 500V
C 7	1	305-20-12000	600	CAP. 1200PF 1% 500V
C 8	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 9	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 10	1	304-13-05609	600	CAP. 56PF 1% 500V
C 11	1	304-08-04709	600	CAP. 47PF .5PF 500V
C 12	1	336-14-10003	601	CAP. 1.0MF 10% 35V
CR 1	6	088-10-09140		DIODE,SWITCH,75V,TRR 4NS/
THRU				
CR 6				
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	1	263-10-49380		XSTR,PNP DUAL 40V AMPL
Q 2	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 3	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 4	1	263-16-00219		XSTR,DUAL PNP,LL DIFF AMP
Q 6	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 7	1	263-10-39560		XSTR,FET N CHAN,MATCHED
Q 8	1	263-99-00419	13369	XSTR,FET,N CHANNEL
Q 9	1	263-10-39560		XSTR,FET N CHAN,MATCHED
Q 10	1	263-10-43920		XSTR,SI FET,N CHAN,SWITCH
Q 11	3	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
THRU				
Q 13				
Q 14	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 15	3	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
THRU				
Q 17				
Q 18	1	263-97-49170		XSTR,PNP SWITCH/AMPL 30V
Q 19	1	263-10-08340		XSTR,NPN 350MHZ SW,ON 35N
Q 20	1	263-97-49170		XSTR,PNP SWITCH/AMPL 30V
R 1	1	608-09-24901	624	RES, 24.9K 1% 1/10W
R 2	1	616-02-10000		RES,1K 5% 1/4W

Table 6-11 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 3	1	608-09-24901	624	RES, 24.9K 1% 1/10W
R 4	1	608-09-75001	624	RES, 75.0K 1% 1/10W
R 5	1	608-09-88700	624	RES, 8.87K 1% 1/10W
R 6	1	608-09-24901	624	RES, 24.9K 1% 1/10W
R 7	1	608-09-24901	624	RES, 24.9K 1% 1/10W
R 8	1	616-02-10000		RES,1K 5% 1/4W
R 9	1	608-09-75001	624	RES, 75.0K 1% 1/10W
R 10	1	608-09-88700	624	RES, 8.87K 1% 1/10W
R 11	1	616-02-51000		RES,5.1K 5% 1/4W
R 12	1	616-02-10000		RES,1K 5% 1/4W
R 13	1	616-02-22009		RES,220 OHM 5% 1/4W
R 14	1	616-02-04709		RES,47 OHM 5% 1/4W
R 15	1	616-02-04709		RES,47 OHM 5% 1/4W
R 16	1	608-09-31600	624	RES. 3.16K 1% 1/10W
R 17	1	648-01-50000		RES, 5.0K .01% .3W
R 18	1	648-01-50000		RES, 5.0K .01% .3W
R 19	1	608-09-17401	624	RES, 17.4K 1% 1/10W
R 20	1	608-09-17401	624	RES, 17.4K 1% 1/10W
R 21	1	608-09-27401	624	RES, 27.4K 1% 1/10W
R 22	1	608-09-24901	624	RES, 24.9K 1% 1/10W
R 23	1	608-09-49900	624	RES. 4.99K 1% 1/10W
R 24	1	608-09-17401	624	RES, 17.4K 1% 1/10W
R 25	1	608-09-17401	624	RES, 17.4K 1% 1/10W
R 26	1	608-09-27401	624	RES, 27.4K 1% 1/10W
R 27	1	608-09-24901	624	RES, 24.9K 1% 1/10W
R 28	1	616-02-10000		RES,1K 5% 1/4W
R 30	1	616-02-51000		RES,5.1K 5% 1/4W
R 31	1	608-09-53600	624	RES, 5.36K 1% 1/10W
R 32	1	608-09-10001	624	RES. 10K 1% 1/10W
R 33	1	608-09-60400	624	RES, 6.04K 1% 1/10W
R 34	1	616-02-39000		RES,3.9K 5% 1/4W
R 35	1	616-02-01009		RES,10 OHM 5% 1/4W
R 36	1	616-02-51000		RES,5.1K 5% 1/4W
R 37	1	616-02-22001		RES,22K 5% 1/4W
R 38	1	608-09-13300	624	RES, 1.33K 1% 1/10W
R 39	1	608-09-27400	624	RES. 2.74K 1% 1/10W
R 40	1	608-09-10000	624	RES. 1K 1% 1/10W
R 41	1	616-02-39001		RES,39K 5% 1/4W
TP 1	1	143-98-00037		JACK,TEST BLACK .46 X.23
TP 2	1	143-98-00037		JACK,TEST BLACK .46 X.23
REF 1	1	905-01-00634	18843	SCHEMATIC,PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

Table 6-12

E M R - T E L E M E T R Y

PARTS LIST 22852 REV DATE REV LTR

LIST TITLE PWA,FRAME SYNC RECOG CHG CONT NO. CODE IDENT 06141 SHT 1 OF 2
PART NO. 205-89-01272 ECO CKD BY Brown

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00867	22851	PWB,FRAME SYNC RECOG
2	6	189-99-00005		8 PIN * USE OPTL * TO-5,0.075 HIGH
C 1	1	337-14-33003	601	CAP. 3.3MF 10% 35V
C 2	1	337-14-33003	601	CAP. 3.3MF 10% 35V
C 3	1	301-13-10003		CAP., 1.0MF 20% 50V LS.20
C 4	1	304-41-82009	600	CAP. 820PF 1% 300V
C 5	1	337-14-33003	601	CAP. 3.3MF 10% 35V
R 1	1	605-09-10000	625	RES. 1K 1% 1/8W
R 2	1	605-09-03329	625	RES. 33.2 OHM 1% 1/8W
R 3	1	605-09-10509	625	RES. 105 OHM 1% 1/8W
R 4	1	605-09-10709	625	RES. 107 OHM 1% 1/8W
R 5	1	605-09-09769	625	RES. 97.6 OHM 1% 1/8W
R 6	1	605-09-49909	625	RES. 499 OHM 1% 1/8W
R 7	1	605-09-15009	625	RES. 150 OHM 1% 1/8W
R 8	1	605-09-82509	625	RES. 825 OHM 1% 1/8W
R 9	1	616-02-10000		RES,1K 5% 1/4W

FIRST MODEL USAGE 0515

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
TP 1 THRU TP 3	3	143-98-00005		JACK, TEST
P 1	1	063-98-00162		CONN, RECP, 52 POSN .150 SP
U 1 THRU U 6	6	046-34-00006		INTCKT, VOLTAGE COMPARATOR
U 7	1	046-97-00075		INTCKT, MONOSTABLE MULTI
U 8 THRU U 10	3	046-97-00073		INTCKT, 5 BIT SHIFT REG
U 11	1	046-97-00047		INTCKT, HEX INVERTERS
U 12	1	046-97-00057		INTCKT, DUAL 2 WIDE 2 IN
U 13	1	046-97-00057		INTCKT, DUAL 2 WIDE 2 IN
U 14	1	046-97-00054		INTCKT, 8 IN POS NAND GATE
U 15	1	046-97-00047		INTCKT, HEX INVERTERS
U 16	1	046-97-00047		INTCKT, HEX INVERTERS
U 17	1	046-97-00044		INTCKT, QUAD, 2 INPUT POS
REF 1	1	905-01-00914	22850	SCHEMATIC, PWA FRAME SYNC
REF 2	1	905-04-~~00002~~ 00001	9500	SPEC, COMPONENT SPACING
			FIRST MODEL USAGE	0515

Table 6-13

PARTS LIST 22066 REV DATE 08/09/74 REV LTR B

LIST TITLE PWA,CHAN/FRAME COUNTER CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. 205-89-01029 ECO 49764 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00671	22065	PWB,CHAN/FRAME COUNTER
2	1	189-98-00004		PAD,XSTR 4 PIN*USE OPTL*
C 1	1	336-12-33003	601	CAP., 3.3MF 10% 15V
C 2	1	304-20-10009	600	CAP. 100PF 1% 500V
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
R 1	1	616-02-27009		RES,270 OHM 5% 1/4W
R 2	1	616-02-12001		RES,12K 5% 1/4W
R 3	1	616-02-51009		RES,510 OHM 5% 1/4W
R 4	1	616-02-47009		RES,470 OHM 5% 1/4W
R 5	1	616-02-47000		RES,4.7K 5% 1/4W
R 6	1	616-02-22000		RES,2.2K 5% 1/4W
TP 1	1	143-98-00005		JACK,TEST,BLACK
TP 2	1	143-98-00005		JACK,TEST,BLACK
U 1	1	046-97-00044		INTCKT,QUAD,2 INPUT POS
U 2	1	046-97-00047		INTCKT,HEX INVERTERS
U 3	1	046-97-00064		INTCKT,DUAL EDGE TRIGGER
U 4	1	046-97-00044		INTCKT,QUAD,2 INPUT POS
U 5	1	046-97-00050		INTCKT,TRIPLE 3 IN POS
U 6	1	046-97-00064		INTCKT,DUAL EDGE TRIGGER
U 7	1	046-97-00044		INTCKT,QUAD,2 INPUT POS
U 8	1	046-97-00076		INTCKT,SYNC 4 BIT UP/DOWN
U 9	1	046-97-00076		INTCKT,SYNC 4 BIT UP/DOWN
U 10	1	046-97-00047		INTCKT,HEX INVERTERS
REF 1	1	905-01-00726	22064	SCHEMATIC, CHAN/FR CNTR
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

FIRST USAGE MODEL 517

EDC

Table 6-14 E M R - T E L E M E T R Y

PARTS LIST 22063 REV DATE 06/23/71 REV LTR B

LIST TITLE PWA, CLOCK GENERATOR CHGE CONT NO. CODE IDENT SHT 1 OF 2
PART NO. 205-89-01028 ECO 42539 06141 CKD BY Brown

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00670	22062	PWB, CLOCK GENERATOR
C 1	1	304-20-10009	600	CAP. 100PF 1% 500V
C 2	1	304-20-27009	600	CAP. 270PF 1% 500V
C 3	1	304-20-20009	600	CAP. 200PF 1% 500V
C 4	1	336-12-33003	601	CAP., 3.3MF 10% 15V
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
R 1 THRU R 5	5	616-02-12001		RES,12K 5% 1/4W
R 6	1	616-02-27009		RES,270 OHM 5% 1/4W
R 7 THRU R 9	3	616-02-51009		RES,510 OHM 5% 1/4W
R 10 THRU R 12	3	616-02-47009		RES,470 OHM 5% 1/4W
R 13	1	616-02-16001		RES,16K 5% 1/4W
R 14	1	616-02-16001		RES,16K 5% 1/4W

FIRST USAGE MODEL 517

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
TP 1	1	143-98-00005		JACK, TEST
TP 2	1	143-98-00005		JACK, TEST
U 1	1	046-97-00047		INTCKT,HEX INVERTERS
U 2	1	046-97-00058		INTCKT,EXP 4 WIDE 2 IN
U 3	1	046-97-00060		INTCKT,DUAL 4 IN EXPANDER
U 4	1	046-97-00047		INTCKT,HEX INVERTERS
U 5	1	046-97-00064		INTCKT,DUAL EDGE TRIGGER
U 6	1	046-97-00044		INTCKT,QUAD,2 INPUT POS
U 7	1	046-97-00044		INTCKT,QUAD,2 INPUT POS
U 8 THRU U 11	4	046-97-00069		INTCKT,DECADE COUNTERS
REF 1	1	905-01-00725	22061	SCHEMATIC, PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

FIRST USAGE MODEL 517

Table 6-15

PARTS LIST 18854 REV DATE 03/14/74 REV LTR C

LIST TITLE PWA,VCO CHGE CONT NO. CODE IDENT SHT 1 OF 3

PART NO. 205-89-00877 ECO RECORD 1 06141 CKD BY Brian

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00585	18853	PWB,VCC
2	31	189-98-00004		PAD,XSTR 4 PIN*USE CPTL*
3	1	189-99-00005	800-3	PAD,XSTR 8 PIN*USE CPTL*
C 1	1	304-20-10009	600	CAP. 100PF 1% 500V
C 2	1	304-20-10009	600	CAP. 100PF 1% 500V
C 3	3	336-14-10003	601	CAP. 1.0MF 10% 35V
THRU				
C 5				
C 6	1	336-12-33003	601	CAP., 3.3MF 10% 15V
CR 2	1	088-99-00129	642-05	DIODE,1N751A ZENER 5.1V
CR 3	1	088-10-09140		DIODE,SWITCH,75V,TRR 4NS/
CR 4	1	088-99-00129	642-05	DIODE,1N751A ZENER 5.1V
CR 5	5	088-10-09140		DIODE,SWITCH,75V,TRR 4NS/
THRU				
CR 9				
P 1	1	063-98-00162		CONN,RECP,52 PCSN .150 SP
Q 1	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 2	1	263-99-00099	801	XSTR,NPN 20V SW,350 MHZ
Q 3	1	263-99-00099	801	XSTR,NPN 20V SW,350 MHZ
Q 4	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 5	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 6	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 7	25	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
THRU				
Q 31				
R 1	1	616-02-10001		RES,10K 5% 1/4W
R 2	1	616-02-15000		RES,1.5K 5% 1/4W
R 3	1	616-02-27001		RES,27K 5% 1/4W
R 4	1	616-02-27000		RES,2.7K 5% 1/4W
R 5	1	616-02-91009		RES,910 OHM 5% 1/4W
R 6	1	201-98-00029		POT. 200 OHM 10% 1W
R 7	1	616-02-27000		RES,2.7K 5% 1/4W
R 8	1	616-02-27001		RES,27K 5% 1/4W
R 9	1	616-02-15000		RES,1.5K 5% 1/4W
R 10	1	616-02-39000		RES,3.9K 5% 1/4W
R 11	1	616-02-39000		RES,3.9K 5% 1/4W
R 12	1	616-02-27000		RES,2.7K 5% 1/4W
R 13	1	616-02-27000		RES,2.7K 5% 1/4W
R 14	1	616-02-47001		RES,47K 5% 1/4W
R 15	1	616-02-47000		RES,4.7K 5% 1/4W

NO.	REQD	NUMBER	SPEC NO.	
R 16	1	616-02-01509		RES,15 OHM 5% 1/4W
R 17	1	616-02-01509		RES,15 OHM 5% 1/4W
R 18	1	616-02-27000		RES,2.7K 5% 1/4W
R 19	1	605-12-40001	625	RES, 40K .1% 1/8W
R 20	1	605-12-40001	625	RES, 40K .1% 1/8W
R 21	1	605-12-20001	625	RES, 20K .1% 1/8W
R 22	1	605-12-20001	625	RES, 20K .1% 1/8W
R 23	1	605-12-10001	625	RES., 10K .1% 1/8W
R 24	1	605-12-10001	625	RES., 10K .1% 1/8W
R 25	1	605-12-50000	625	RES, 5K .1% 1/8W
R 26	1	605-12-50000	625	RES, 5K .1% 1/8W
R 27	1	608-09-40202	624	RES, 402.0K 1% 1/10W
R 28	1	608-09-40202	624	RES, 402.0K 1% 1/10W
R 29	1	608-09-20002	624	RES, 200.0K 1% 1/10W
R 30	1	608-09-20002	624	RES, 200.0K 1% 1/10W
R 31	1	608-09-10002	624	RES, 100.0K 1% 1/10W
R 32	1	608-09-10002	624	RES, 100.0K 1% 1/10W
R 33	1	608-09-49901	624	RES, 49.9K 1% 1/10W
R 34	1	608-09-49901	624	RES, 49.9K 1% 1/10W
R 35	1	616-02-39003		RES,3.9 MEG 5% 1/4W
R 36	1	616-02-39003		RES,3.9 MEG 5% 1/4W
R 37	1	616-02-20003		RES,2 MEG 5% 1/4W
R 38	1	616-02-20003		RES,2 MEG 5% 1/4W
R 39	1	616-02-10003		RES,1 MEG 5% 1/4W
R 40	1	616-02-10003		RES,1 MEG 5% 1/4W
R 41	1	616-02-51002		RES,510K 5% 1/4W
R 42	1	616-02-51002		RES,510K 5% 1/4W
R 51	1	616-02-10002		RES,100K 5% 1/4W
R 52	1	616-02-10002		RES,100K 5% 1/4W
R 53	1	616-02-51001		RES,51K 5% 1/4W
R 54	1	616-02-51001		RES,51K 5% 1/4W
R 55	1	616-02-24001		RES,24K 5% 1/4W
R 56	1	616-02-24001		RES,24K 5% 1/4W
R 57	1	616-02-12001		RES,12K 5% 1/4W
R 58	1	616-02-12001		RES,12K 5% 1/4W
R 59 THRU R 74	16	616-02-10002		RES,100K 5% 1/4W
R 83	1	608-09-59000	624	RES, 5.90K 1% 1/10W
TP 1	1	143-98-00037		JACK,TEST BLACK .46 X.23
TP 2	1	143-98-00037		JACK,TEST BLACK .46 X.23
U 1	1	046-34-00007		INTCKT,VOLTAGE FOLLOWER
U 2	1	046-07-00033		INTCKT,QUAD 2IN NAND GATE
U 3 THRU	3	046-10-00019		INTCKT,HIGH VOLT HEX INV.

Table 6-15 (Cont'd.):

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
REF 1	1	905-04-00001	9500	SPEC,COMPONENT SPACING
REF 2	1	905-01-00638	18852	SCHEMATIC,PWA

Table 6-16
PARTS LIST 18875 REV DATE 10/09/73 REV LTR H

LIST TITLE PWA,LOOP FILTER CHGE CONT NO. CODE IDENT SHT 1 OF 4
PART NO. 205-89-00879 ECO 47653 06141 CKD BY Brown

ITEM NO.	QTY REQD	EMR NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00591	18874	PWB,LOOP FILTER
2	28	189-98-00004		PAD,XSTR 4 PIN*USE CPTL*
3	2	189-99-00005	8CC-3	PAD,XSTR 8 PIN*USE CPTL*
C 1	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 2	1	336-12-33003	601	CAP., 3.3MF 10% 15V
C 3	4	336-14-10003	601	CAP. 1.0MF 10% 35V
THRU				
C 6				
C 7	1	336-12-33003	601	CAP., 3.3MF 10% 15V
C 8	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 9	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 10	1	305-20-33000	600	CAP. 3300PF 1% 500V
C 11	1	336-08-33001		CAP., .033MF 5% 100V
C 12	1	336-05-33002	601	CAP. .33MF 5% 35V
C 13	1	336-05-33003	601	CAP. 3.3MF 5% 35V
C 14	1	337-02-33004	601	CAP., 33MF 5% 10V
C 15	1	339-01-33005	601	CAP., 330MF 5% 6V
C 16	1	304-20-33009	600	CAP. 330PF 1% 500V
C 17	1	305-20-33000	600	CAP. 3300PF 1% 500V
C 18	1	336-08-33001		CAP., .033MF 5% 100V
C 19	1	336-05-33002	601	CAP. .33MF 5% 35V
C 20	1	336-05-33003	601	CAP. 3.3MF 5% 35V
C 21	1	337-02-33004	601	CAP., 33MF 5% 10V
C 22	1	304-20-10009	600	CAP. 100PF 1% 500V
CR 1	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA
CR 2	1	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	3	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
THRU				
Q 3				

FIRST USAGE MODEL 515

Table 6-16 (Cont'd.).

ITEM NO.	QTY RECD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
Q 4	8	263-10-24321		XSTR,NPN LL CHOPPER 45V
THRU				
Q 11				
Q 12	9	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
THRU				
Q 20				
Q 21	8	263-10-24321		XSTR,NPN LL CHOPPER 45V
THRU				
Q 28				
R 1	1	608-09-57601	624	RES, 57.6K 1% 1/10W
R 2	1	608-09-29401	624	RES, 29.4K 1% 1/10W
R 5	4	616-02-10001		RES,10K 5% 1/4W
THRU				
R 8				
R 9	4	616-02-20001		RES,20K 5% 1/4W
THRU				
R 12				
R 13	11	616-02-62000		RES,6.2K 5% 1/4W
THRU				
R 23				
R 24	1	608-09-22101	624	RES, 22.1K 1% 1/10W
R 25	1	608-09-11001	624	RES, 11.0K 1% 1/10W
R 26	1	608-09-54900	624	RES, 5.49K 1% 1/10W
R 27	1	608-09-27400	624	RES. 2.74K 1% 1/10W
R 28	1	608-09-22102	624	RES, 221.0K 1% 1/10W
R 29	1	608-09-11002	624	RES, 110.0K 1% 1/10W
R 30	1	608-09-54901	624	RES, 54.9K 1% 1/10W
R 31	1	608-09-27401	624	RES, 27.4K 1% 1/10W
R 32	1	608-09-57600	624	RES. 5.76K 1% 1/10W
R 33	1	608-09-24309	624	RES, 243.0 OHM 1% 1/10W
R 34	1	608-09-24309	624	RES, 243.0 OHM 1% 1/10W
R 35	1	608-09-40200	624	RES, 4.02K 1% 1/10W
R 36	1	608-09-51100	624	RES, 5.11K 1% 1/10W
R 37	1	608-09-54909	624	RES., 549 OHM 1% 1/10W

FIRST USAGE MODEL 515

Table 6-16 (Cont'd.)

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 38	1	616-02-10001		RES,10K 5% 1/4W
R 39	1	616-02-62000		RES,6.2K 5% 1/4W
R 40	1	616-02-51000		RES,5.1K 5% 1/4W
R 41	1	616-02-22003		RES,2.2 MEG 5% 1/4W
R 42	1	616-02-11003		RES,1.1 MEG 5% 1/4W
R 43	1	608-01-54902	624	RES, 549K 1% 1/10W 100PPM
R 44	1	608-09-27402	624	RES, 274.0K 1% 1/10W
R 45	1	608-09-22101	624	RES, 22.1K 1% 1/10W
R 46	1	608-09-11001	624	RES, 11.0K 1% 1/10W
R 47	1	608-09-54900	624	RES, 5.49K 1% 1/10W
R 48	1	608-09-27400	624	RES. 2.74K 1% 1/10W
R 49	1	608-09-22102	624	RES, 221.0K 1% 1/10W
R 50	1	608-09-11002	624	RES, 110.0K 1% 1/10W
R 51	1	608-09-54901	624	RES, 54.9K 1% 1/10W
R 52	1	608-09-27401	624	RES, 27.4K 1% 1/10W
R 53	1	608-09-24900	624	RES. 2.49K 1% 1/10W
R 54	1	608-09-21500	624	RES. 2.15K 1% 1/10W
R 55	1	201-98-00014		PCT., 500 OHM 10% 1W
R 56	1	608-09-21500	624	RES. 2.15K 1% 1/10W
R 57	1	608-09-16500	624	RES. 1.65K OHM 1% 1/10W
R 58	1	608-09-41200	624	RES, 4.12K 1% 1/10W
R 59	1	608-09-90900	624	RES. 9.09K 1% 1/10W
R 60 THRU R 67	8	616-02-10001		RES,10K 5% 1/4W
R 68 THRU R 71	4	616-02-20001		RES,20K 5% 1/4W
R 72	1	608-09-10000	624	RES. 1K 1% 1/10W
R 73	1	616-02-20009		RES,200 OHM 5% 1/4W
R 74	1	608-09-21501	624	RES, 21.5K 1% 1/10W
R 76	1	616-02-51000		RES,5.1K 5% 1/4W
R 77	1	608-09-49909	624	RES, 499.0 OHM 1% 1/10W
U 1	1	046-18-00015		INTGKT,HIGH VOLT HEX INV.

FIRST USAGE MODEL 515

Table 6-16 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
U 2	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 3	1	046-18-00015		INTCKT,HIGH VOLT HEX INV.
U 4	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 5	1	046-97-00022		INTCKT EXPAND.DUAL 2 IN
U 6	1	046-97-00022		INTCKT EXPAND.DUAL 2 IN
U 7	1	046-18-00015		INTCKT,HIGH VOLT HEX INV.
U 10	1	046-44-00002		INTCKT,OPNL AMPL,FET INP
U 11	1	046-15-00003		INTCKT,3 XSTR AND 1 DIFF
U 13	1	046-34-00007		INTCKT,VOLTAGE FOLLOWER
U 17	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 18	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 19	1	046-34-00002		INTCKT,OPNL AMPL INT COMP
U 20	1	046-15-00003		INTCKT,3 XSTR AND 1 DIFF
REF 1	1	905-01-00645	18873	SCHEMATIC,PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

FIRST USAGE MODEL 515

PARTS LIST 18865 REV DATE 03/14/74 REV LTR E

LIST TITLE PWA,MONOSTABLE CHGE CONT NO. CODE IDENT SHT 1 OF 3

PART NO. 205-89-00880 ECO RECORD 1 06141 CKD BY Brown

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00589	18865	PWB,MONOSTABLE
2	23	189-98-00004		PAD,XSTR 4 PIN*USE CPTL*
3	1	189-98-00016		PAD,XSTR,TO-5 8PIN,.075H
C 1	1	337-05-18003	601	CAP. 1.8MF 5% 35V
C 2	1	336-07-18002		CAP., .18MF 5% 75V
C 3	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 4	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 5	1	336-08-18001		CAP., .018MF 5% 100V
C 6	1	336-12-33003	601	CAP., 3.3MF 10% 15V
C 7	1	305-20-18000	600	CAP. 1800PF 1% 500V
C 8	1	304-20-18009	600	CAP. 180PF 1% 500V
C 9	1	304-20-15009	600	CAP. 150PF 1% 500V
CR 2	1	088-99-00129	642-05	DIODE,1N751A ZENER 5.1V
CR 3	1	088-10-09140		DIODE,SWITCH,75V,TRR 4NS/
CR 4	1	088-99-00129	642-05	DIODE,1N751A ZENER 5.1V
CR 5 THRU CR 7	3	088-10-09140		DIODE,SWITCH,75V,TRR 4NS/
CR 8 THRU CR 13	6	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 2	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 3	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 4	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 5	1	263-10-08340		XSTR,NPN 350MHZ SW,CN 35N
Q 6	1	263-99-00099	801	XSTR,NPN 20V SW,350 MHZ
Q 7	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 8	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 9	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 10	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 11	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 12	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 13	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 14	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 15	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 16	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 17	1	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 18	6	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V

Table 6-17 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 1	1	608-09-10001	624	RES. 10K 1% 1/10W
R 2	1	616-02-15000		RES,1.5K 5% 1/4W
R 3	1	616-02-27001		RES,27K 5% 1/4W
R 4	1	616-02-27000		RES,2.7K 5% 1/4W
R 5	1	616-02-91009		RES,910 OHM 5% 1/4W
R 6	1	201-98-00029		POT. 200 OHM 10% 1W
R 7	1	616-02-15000		RES,1.5K 5% 1/4W
R 8	1	616-02-27001		RES,27K 5% 1/4W
R 9	1	616-02-15000		RES,1.5K 5% 1/4W
R 11	1	616-02-39009		RES,3.9K 5% 1/4W
R 12	1	616-02-27000		RES,2.7K 5% 1/4W
R 13	1	616-02-27000		RES,2.7K 5% 1/4W
R 14	1	616-02-10001		RES,10K 5% 1/4W
R 15	1	616-02-10001		RES,10K 5% 1/4W
R 16	1	616-02-01509		RES,15 OHM 5% 1/4W
R 17	1	616-02-01509		RES,15 OHM 5% 1/4W
R 18	1	616-02-16000		RES,1.6K 5% 1/4W
R 19	1	605-09-40201	625	RES. 40.2K 1% 1/8W
R 20	1	605-09-20001	625	RES. 20K 1% 1/8W
R 21	1	605-09-10001	625	RES. 10.0K 1% 1/8W
R 22	1	605-09-49900	625	RES. 4.99K 1% 1/8W
R 23	1	605-09-40202	625	RES. 402K 1% 1/8W
R 24	1	608-09-20002	624	RES, 200.0K 1% 1/10W
R 25	1	608-09-10002	624	RES, 100.0K 1% 1/10W
R 26	1	608-09-49901	624	RES, 49.9K 1% 1/10W
R 27	1	616-02-39003		RES,3.9 MEG 5% 1/4W
R 28	1	616-02-20003		RES,2 MEG 5% 1/4W
R 29	1	616-02-10003		RES,1 MEG 5% 1/4W
R 30	1	616-02-51002		RES,51CK 5% 1/4W
R 31	1	616-02-10002		RES,100K 5% 1/4W
R 32	1	616-02-51001		RES,51K 5% 1/4W
R 33	1	616-02-24001		RES,24K 5% 1/4W
R 34	1	616-02-12001		RES,12K 5% 1/4W
R 35 THRU R 42	8	616-02-10002		RES,100K 5% 1/4W
R 44	1	616-02-56001		RES,56K 5% 1/4W
R 45	1	616-02-56001		RES,56K 5% 1/4W
R 47	1	616-02-56001		RES,56K 5% 1/4W
R 49	1	616-02-56001		RES,56K 5% 1/4W
R 51	1	616-02-56001		RES,56K 5% 1/4W
R 53	1	608-09-71500	624	RES. 7.15K 1% 1/10W
R 54 THRU	12	616-02-20000		RES,2K 5% 1/4W

ECO 1

Table 6-17 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
TP 1	1	143-98-00037		JACK,TEST BLACK .46 X.23
TP 2	1	143-98-00037		JACK,TEST BLACK .46 X.23
U 1	1	046-34-00007		INTCKT,VOLTAGE FOLLOWER
U 2	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 3 THRU U 5	3	046-18-00015		INTCKT,HIGH VOLT HEX INV.
REF 1	1	905-01-00643	18864	SCHEMATIC,PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

Table 6-18

PARTS LIST 18857 REV DATE 03/14/74 REV LTR G

LIST TITLE PWA,DIFFERENTIATOR CHGE CONT NO. CODE IDENT SHT 1 OF 2

PART NO. 205-99-00874 ECO RECORD 1 06141 CKD BY Brian

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00582	18856	PWB,DIFFERENTIATOR
2	5	189-99-00005	800-3	PAD,XSTR 8 PIN*USE CPTL*
3	16	189-98-00004		PAD,XSTR 4 PIN*USE CPTL*
C 1	1	304-20-18009	600	CAP. 18PF 1% 500V
C 2	1	336-04-18003	601	CAP. 1.8MF 5% 20V
C 3	1	336-07-18002		CAP., .18MF 5% 75V
C 4	1	336-08-18001		CAP., .018MF 5% 100V
C 5	1	305-20-16000	600	CAP. 160PF 1% 500V
C 6	1	336-13-22003	601	CAP. 2.2MF 10% 20V
C 7	1	336-13-22003	601	CAP. 2.2MF 10% 20V
C 9	1	336-13-22003	601	CAP. 2.2MF 10% 20V
C 10	1	336-12-33003	601	CAP., 3.3MF 10% 15V
C 11	1	304-62-10000	600	CAP. 1000PF 1% 100V
C 12	1	304-62-10000	600	CAP. 1000PF 1% 100V
C 13	1	336-12-33003	601	CAP., 3.3MF 10% 15V
C 14	1	336-13-22003	601	CAP. 2.2MF 10% 20V
C 15	1	337-13-10004	601	CAP., 10MF 10% 20V
CR 3	1	088-10-41480		DIODE,SW,75V/50A,4NS/10MA
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1 THRU Q 4	4	263-10-29451		XSTR,PNP LL CHOPPER HFE
Q 5 THRU Q 12	8	263-38-00019		XSTR,FET P CHAN CHOPPER
Q 13 THRU Q 16	4	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
R 1	1	616-02-10001		RES,10K 5% 1/4W
R 2	1	616-02-30000		RES,3K 5% 1/4W
R 3	1	616-02-15000		RES,1.5K 5% 1/4W
R 4	1	616-02-68009		RES,680 OHM 5% 1/4W
R 5	1	616-02-27009		RES,270 OHM 5% 1/4W
R 6	1	616-02-30001		RES,30K 5% 1/4W
R 7	1	616-02-15001		RES,15K 5% 1/4W
R 8	1	616-02-75000		RES,7.5K 5% 1/4W
R 9	1	616-02-36000		RES,3.6K 5% 1/4W
R 11	1	608-01-47502	624	RES, 475K 1% 1/10W 100 PP
R 12	1	608-01-47502	624	RES, 475K 1% 1/10W 100 PP
R 13	1	608-09-10001	624	RES. 10K 1% 1/10W

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 14	1	201-98-00014		POT., 500 OHM 10% 1W
R 15	1	608-09-10001	624	RES. 10K 1% 1/10W
R 16	1	608-09-10001	624	RES. 10K 1% 1/10W
R 17	1	201-98-00014		POT., 500 OHM 10% 1W
R 18	1	608-09-10001	624	RES. 10K 1% 1/10W
R 20	4	616-02-47000		RES,4.7K 5% 1/4W
THRU				
R 23				
R 24	8	616-02-75000		RES,7.5K 5% 1/4W
THRU				
R 31				
R 32	1	616-02-33009		RES,330 OHM 5% 1/4W
R 33	1	616-02-33009		RES,330 OHM 5% 1/4W
R 34	3	616-02-47000		RES,4.7K 5% 1/4W
THRU				
R 36				
R 37	1	616-02-10000		RES,1K 5% 1/4W
R 38	1	201-98-00138		POT., 1K 10% .75W PC MTG
R 39	1	616-02-10000		RES,1K 5% 1/4W
R 40	1	616-02-47000		RES,4.7K 5% 1/4W
R 41	1	616-02-75009		RES,750 OHM 5% 1/4W
R 42	1	616-02-10002		RES,100K 5% 1/4W
R 43	1	616-02-33000		RES,3.3K 5% 1/4W
R 44	1	616-02-51000		RES,5.1K 5% 1/4W
TP 1	3	143-98-00037		JACK,TEST BLACK .46 X.23
THRU				
TP 3				
U 1	1	046-34-00007		INTCKT,VOLTAGE FOLLOWER
U 2	1	046-34-00007		INTCKT,VOLTAGE FOLLOWER
U 3	1	046-34-00006		IC,VOLTAGE COMPTR,DIFF
U 4	1	046-34-00006		IC,VOLTAGE COMPTR,DIFF
U 5	1	046-18-00015		INTCKT,HIGH VOLT HEX INV.
U 6	1	046-18-00015		INTCKT,HIGH VOLT HEX INV.
U 7	4	046-97-00034		INTCKT,QUAD 2IN NAND GATE
THRU				
U 10				
U 11	1	046-97-00201		IC,OPNL AMPL +-18V 0-70*C
U 12	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
REF 1	1	905-01-00635	18855	SCHEMATIC,PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

Table 6-19

PARTS LIST 21808 REV DATE 03/14/74 REV LTR D

LIST TITLE PWA, PAM/PDM CONVERTER CHGE CONT NO. CODE IDENT SHT 1 OF 3

PART NO. 205-89-01016 ECO RECORD 1 06141 CKD BY Brown

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00668	21807	PWB,PDM CONVERTER
2	32	189-99-00003	800-7	PAD,XSTR 4 PIN*USE OPTL*
3	3	189-99-00005	800-3	PAD,XSTR 8 PIN*USE OPTL*
C 1	8	301-13-10002		CAP., .1MF 20% 50V LS.200
THRU				
C 8				
C 9	1	304-20-33009	600	CAP. 330PF 1% 500V
C 10	1	304-01-01509	600	CAP. 15PF .5PF 500V
C 11	1	707-01-82002	904	CAP., .8200MF 1% 50V
C 12	1	384-05-82001	949	CAP., .0820MF 1% 50V
C 13	1	384-05-73600	949	CAP., 7360PF 1% 50V
C 14	1	304-41-82009	600	CAP. 820PF 1% 300V
C 15	1	301-13-47002		CAP., .47MF 20% 50V LS.20
C 16	1	301-03-47001		CAP., .047MF 20% 50V LS.1
C 17	1	301-05-47000		CAP.,4700PF 10% 100V
C 18	1	304-20-47009	600	CAP. 470PF 1% 500V
C 19	1	301-13-10002		CAP., .1MF 20% 50V LS.200
C 20	1	336-12-33003	601	CAP., 3.3MF 10% 15V
CR 1	1	088-99-00299	642-09	DIODE,1N755A ZENER 7.5V
CR 2	3	088-10-41480		DIODE,SW,75V/5UA,4NS/10MA
THRU				
CR 4				
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	22	263-16-00229		XSTR,P CHAN DEPLET MODE
THRU				
Q 22				
Q 23	1	263-45-00019		XSTR,MOSFET P CHAN 30V SW
Q 24	4	263-10-43920		XSTR,SI FET,N CHAN,SWITCH
THRU				
Q 27				
Q 28	4	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
THRU				
Q 31				
Q 32	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
R 1	1	608-09-11001	624	RES, 11.0K 1% 1/10W
R 2	1	608-09-22601	624	RES, 22.6K 1% 1/10W
R 3	1	608-09-45301	624	RES, 45.3K 1% 1/10W
R 4	1	608-09-90901	624	RES, 90.9K 1% 1/10W
R 5	1	608-09-11302	624	RES, 113.0K 1% 1/10W
R 6	1	608-09-22602	624	RES, 226.0K 1% 1/10W

EDC

Table 6-19 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 7	1	608-01-45302	624	RES, 453K 1% 1/10W 100 PP
R 8	1	608-01-90902	624	RES, 909K 1% 1/10W 100 PP
R 9	1	616-02-82009		RES,820 OHM 5% 1/4W
R 10	1	616-02-18000		RES,1.8K 5% 1/4W
R 11	1	616-02-39000		RES,3.9K 5% 1/4W
R 12	1	616-02-82000		RES,8.2K 5% 1/4W
R 13	1	616-02-10001		RES,10K 5% 1/4W
R 14	1	616-02-20001		RES,20K 5% 1/4W
R 15	1	616-02-39001		PES,39K 5% 1/4W
R 16	1	616-02-82001		RES,82K 5% 1/4W
R 17	1	608-09-14701	624	RES., 14.7K 1% 1/10W
R 18	1	608-09-51100	624	RES, 5.11K 1% 1/10W
R 19	1	201-98-00040		POT., 20K 10% 1W
R 20	1	608-09-78700	624	RES, 7.87K 1% 1/10W
R 21	1	608-09-20001	624	RES. 20K 1% 1/10W
R 22	1	608-01-40200	624	RES, 4.02K
R 23	1	201-98-00040		POT., 20K 10% 1W
R 24	1	608-09-20001	624	RES. 20K 1% 1/10W
R 25 THRU R 40	16	616-02-18002		RES,180K 5% 1/4W
R 41	1	616-02-47000		RES,4.7K 5% 1/4W
R 42	1	616-02-20001		RES,20K 5% 1/4W
R 43 THRU R 45	3	616-02-22000		RES,2.2K 5% 1/4W
R 46	1	616-02-20003		RES,2 MEG 5% 1/4W
R 47	1	616-02-18002		RES,180K 5% 1/4W
R 48	1	608-09-24900	624	RES, 2.49K 1% 1/10W
R 49	1	608-09-82500	624	RES, 8.25K 1% 1/10W
R 50	1	608-09-17800	624	RES. 1.78K 1% 1/10W
R 51	1	616-02-47000		RES,4.7K 5% 1/4W
R 52	1	616-02-47002		RES,470K 5% 1/4W
R 53	1	616-02-47000		RES,4.7K 5% 1/4W
R 54	1	616-02-82000		RES,8.2K 5% 1/4W
R 55	1	616-02-10001		RES,10K 5% 1/4W
R 56	1	616-02-18002		RES,180K 5% 1/4W
R 57	1	616-02-18002		RES,180K 5% 1/4W
R 58 THRU R 61	4	616-02-10002		RES,100K 5% 1/4W
R 62	1	616-02-18002		RES,180K 5% 1/4W
R 63	1	616-02-18002		RES,180K 5% 1/4W
R 64	1	616-02-10001		RES,10K 5% 1/4W

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 65	1	616-02-51001		RES,51K 5% 1/4W
R 66	1	616-02-51001		RES,51K 5% 1/4W
R 67	1	616-02-47000		RES,4.7K 5% 1/4W
R 68	1	616-02-24001		RES,24K 5% 1/4W
R 69	1	616-02-15002		RES,150K 5% 1/4W
R 70	1	616-02-10001		RES,10K 5% 1/4W
R 71	1	616-02-10001		RES,10K 5% 1/4W
TP 1 THRU TP 3	3	143-98-00005		JACK,TEST,BLACK
U 1	1	046-97-00044		INTCKT,QUAD,2 INPUT POS
U 2	1	046-18-00015		INTCKT,HIGH VOLT HEX INV.
U 3	1	046-18-00015		INTCKT,HIGH VOLT HEX INV.
U 4	1	046-34-00002		INTCKT,OPNL AMPL INT COMP
U 5	1	046-34-00002		INTCKT,OPNL AMPL INT COMP
U 6	1	046-97-00207		IC,DIFF.COMPTR GAIN 1250
U 7	1	046-34-00012		INTCKT,VOLTAGE FOLLOWER
REF 1	1	905-01-00720	21806	PWA,SCHEMATIC PDM CONVERT
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

SPEEDIFLOW® MOORE BUSINESS FORMS, INC. © PATENTED J

Table 6-20

PARTS LIST 18863 REV DATE 05/13/74 REV LTR J

LIST TITLE PWA,INPUT FILTER CHGE CONT NO. CODE IDENT SHT 1 OF 3

PART NO. 205-89-00881 ECO 49587 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00590	18862	PWB,INPUT FILTER
2	12	189-98-00004		PAD,XSTR 4 PIN*USE OPTL*
3	3	189-99-00005	800-3	PAD,XSTR 8 PIN*USE OPTL*
4	AR	276-99-00009	619-24	WIRE,#24,BUSS,SOLID
5	AR	268-02-00049		TUBING,#24,EXTR TEF,CLEAR
C 1	1	336-05-10003	601	CAP. 1.0MF 5% 35V
C 2	1	336-07-10002		CAP., .1MF 5% 75V
C 3	1	384-05-10001	949	CAP., .0100MF 1% 50V
C 4	1	304-62-10000	600	CAP. 1000PF 1% 100V
C 5	1	304-08-03009	600	CAP. 30PF .5PF 500V
C 6	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 7	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 8	1	301-13-47002		CAP., .47MF 20% 50V LS.20
C 9	1	301-03-47001		CAP., .047MF 20% 50V LS.1
C 10	1	301-05-47000		CAP.,470CPF 10% 100V
C 11	1	304-20-47009	600	CAP. 470PF 1% 500V
C 12	1	304-12-05009	600	CAP., 50PF 2% 500V
C 13	4	336-14-10003	601	CAP. 1.0MF 10% 35V
THRU				
C 16				
C 17	1	336-05-10003	601	CAP. 1.0MF 5% 35V
C 18	1	336-07-10002		CAP., .1MF 5% 75V
C 19	1	384-05-10001	949	CAP., .0100MF 1% 50V
C 20	1	304-62-10000	600	CAP. 1000PF 1% 100V
C 21	1	304-01-01509	600	CAP. 15PF .5PF 500V
C 22	1	336-14-10003	601	CAP. 1.0MF 10% 35V
C 23	1	336-12-33003	601	CAP., 3.3MF 10% 15V
CR 1	1	088-16-00089		DIODE,CURRENT LIMITING
CR 2	1	088-16-00099		DIODE,CURRENT LIMITING
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	12	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
THRU				
Q 12				
R 1	1	608-09-10701	624	RES, 10.7K 1% 1/10W
R 2	1	608-09-53600	624	RES, 5.36K 1% 1/10W
R 3	1	608-09-26700	624	RES, 2.67K 1% 1/10W
R 4	1	608-09-13300	624	RES, 1.33K 1% 1/10W
R 5	1	608-09-10702	624	RES, 107.0K 1% 1/10W
R 6	1	608-09-53601	624	RES, 53.6K 1% 1/10W
R 7	1	608-09-26701	624	RES, 26.7K 1% 1/10W

Table 6-20 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 8	1	608-09-13301	624	RES, 13.3K 1% 1/10W
R 9	1	616-02-20009		RES,200 OHM 5% 1/4W
R 10	1	616-02-82009		RES,820 OHM 5% 1/4W
R 11	1	616-02-51000		RES,5.1K 5% 1/4W
R 12	1	608-09-14301	624	RES, 14.3K 1% 1/10W
R 13	1	608-09-71500	624	RES. 7.15K 1% 1/10W
R 14	1	608-09-36500	624	RES, 3.65K 1% 1/10W
R 15	1	608-09-18200	624	RES, 1.82K 1% 1/10W
R 16	1	608-09-14302	624	RES, 143.0K 1% 1/10W
R 17	1	608-09-71501	624	RES. 71.5K 1% 1/10W
R 18	1	608-09-36501	624	RES. 36.5K 1% 1/10W
R 19	1	608-09-18201	624	RES, 18.2K 1% 1/10W
R 20 THRU R 24	5	616-02-10001		RES,10K 5% 1/4W
R 25	1	616-02-20009		RES,200 OHM 5% 1/4W
R 26	1	616-02-82009		RES,820 OHM 5% 1/4W
R 27	1	616-02-51000		RES,5.1K 5% 1/4W
R 28	1	608-09-14301	624	RES, 14.3K 1% 1/10W
R 29	1	608-09-71500	624	RES. 7.15K 1% 1/10W
R 30	1	608-09-34800	624	RES, 3.48K 1% 1/10W
R 31	1	608-09-17400	624	RES, 1.74K 1% 1/10W
R 32	1	608-09-14302	624	RES, 143.0K 1% 1/10W
R 33	1	608-09-71501	624	RES. 71.5K 1% 1/10W
R 34	1	608-09-34801	624	RES. 34.8K 1% 1/10W
R 35	1	608-09-17401	624	RES, 17.4K 1% 1/10W
R 36	1	201-98-00015		POT., 1K 10% 1W
R 37	1	616-02-51000		RES,5.1K 5% 1/4W
R 38	1	616-02-68000		RES,6.8K 5% 1/4W
R 39	1	616-02-33000		RES,3.3K 5% 1/4W
R 44	1	616-02-10001		RES,10K 5% 1/4W
R 45	1	616-02-22001		RES,22K 5% 1/4W
R 46	1	616-02-10001		RES,10K 5% 1/4W
R 47	1	616-02-47000		RES,4.7K 5% 1/4W
R 48	1	616-02-24000		RES,2.4K 5% 1/4W
R 49	1	616-02-62001		RES,62K 5% 1/4W
R 50	1	616-02-43001		RES,43K 5% 1/4W
R 51	1	616-02-22001		RES,22K 5% 1/4W
R 52	1	616-02-10001		RES,10K 5% 1/4W
R 53	1	616-02-30001		RES,30K 5% 1/4W
R 54	1	616-02-15001		RES,15K 5% 1/4W
R 55	1	616-02-62000		RES,6.2K 5% 1/4W
R 56	1	616-02-33000		RES,3.3K 5% 1/4W
R 57	1	616-02-62001		RES,62K 5% 1/4W

Table 6-20 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 58	1	616-02-56001		RES,56K 5% 1/4W
R 59	1	616-02-30001		RES,30K 5% 1/4W
R 60	1	616-02-15001		RES,15K 5% 1/4W
R 61	1	616-02-30001		RES,30K 5% 1/4W
R 62	1	616-02-15001		RES,15K 5% 1/4W
R 63	1	616-02-62000		RES,6.2K 5% 1/4W
R 64	1	616-02-33000		RES,3.3K 5% 1/4W
R 65	1	616-02-62001		RES,62K 5% 1/4W
R 66	1	616-02-56001		RES,56K 5% 1/4W
R 67	1	616-02-30001		RES,30K 5% 1/4W
R 68	1	616-02-15001		RES,15K 5% 1/4W
R 69	1	616-02-36000		RES,3.6K 5% 1/4W
R 70 THRU R 74	5	616-02-51009		RES,510 OHM 5% 1/4W
R 75 THRU R 79	5	616-02-10000		RES,1K 5% 1/4W
R 80	1	616-02-51000		RES,5.1K 5% 1/4W
U 1	1	046-15-00003		INTCKT,3 XSTR AND 1 DIFF
U 2	1	046-34-00007		INTCKT,VOLTAGE FOLLOWER
U 3	1	046-15-00003		INTCKT,3 XSTR AND 1 DIFF
U 4	1	046-15-00003		INTCKT,3 XSTR AND 1 DIFF
U 5	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 6	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 7	1	046-34-00007		INTCKT,VOLTAGE FOLLOWER
U 8	1	046-18-00015		INTCKT,HIGH VOLT HEX INV.
U 9	1	046-97-00033		INTCKT,QUAD 2IN NAND GATE
U 10	1	046-18-00015		INTCKT,HIGH VOLT HEX INV.
U 11	1	046-18-00015		INTCKT,HIGH VOLT HEX INV.
U 12	1	046-97-00034		INTCKT,QUAD 2IN NAND GATE
U 13	1	046-15-00003		INTCKT,3 XSTR AND 1 DIFF
U 14	1	046-34-00007		INTCKT,VOLTAGE FOLLOWER
U 15	1	046-15-00003		INTCKT,3 XSTR AND 1 DIFF
U 16	1	046-15-00003		INTCKT,3 XSTR AND 1 DIFF
REF 1	1	905-01-00644	18861	SCHEMATIC,PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

Table 6-21

PARTS LIST 18883 REV DATE 03/14/74 REV LTR J

LIST TITLE PWA,INPUT AMPLIFIER CHGE CONT NO. CODE IDENT SHT 1 OF 2

PART NO. 205-89-00878 ECO RECORD 1 06141 CKD BY Brown

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00586	18882	PWB,INPUT AMPLIFIER
2	6	189-98-00004		PAD,XSTR 4 PIN*USE CPTL*
3	1	189-98-00030		PAD,XSTR TO-18 8 PIN
4	2	189-98-00005		PAD,XSTR TO-5,9 CR 11,6 P
C 1	1	337-14-33003	601	CAP. 3.3MF 10% 35V
C 2	1	337-14-33003	601	CAP. 3.3MF 10% 35V
C 3	1	301-13-10002		CAP., .1MF 20% 50V LS.200
C 4	1	304-20-10009	600	CAP. 100PF 1% 500V
C 5	1	304-01-00109	600	CAP. 1PF .5PF 500V
C 6	1	305-20-47000	600	CAP. 4700PF 1% 500V
C 7	1	305-20-47000	600	CAP. 4700PF 1% 500V
C 8	1	304-01-00509	600	CAP. 5PF .5PF 500V
C 9	1	301-13-10002		CAP., .1MF 20% 50V LS.200
C 10	1	301-13-10002		CAP., .1MF 20% 50V LS.200
CR 1 THRU CR 4	4	088-10-09140		DIODE,SWITCH,75V,TRR 4NS/
CR 5	1	088-99-00259	642-12	DIODE,1N758A ZENER 10.0V
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	1	263-10-39560		XSTR,FET N CHAN,MATCHED
Q 2	1	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 3	1	263-10-49380		XSTR,PNP DUAL 40V AMPL
Q 4 THRU Q 7	4	263-10-39470		XSTR,NPN 40V SW-AMPL,HFE
Q 8	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 9	1	263-10-39560		XSTR,FET N CHAN,MATCHED
R 1	1	608-09-24901	624	RES, 24.9K 1% 1/10W
R 2	1	608-09-24901	624	RES, 24.9K 1% 1/10W
R 3	1	608-09-88700	624	RES, 8.87K 1% 1/10W
R 4	1	616-02-10009		RES,100 OHM 5% 1/4W
R 5	1	608-09-25501	624	RES, 25.5K 1% 1/10W
R 6	1	616-02-18000		RES,1.8K 5% 1/4W
R 7	1	616-02-04709		RES,47 OHM 5% 1/4W
R 8	1	608-09-12101	624	RES, 12.1K 1% 1/10W
R 9	1	608-09-12101	624	RES, 12.1K 1% 1/10W
R 10	1	608-09-25501	624	RES, 25.5K 1% 1/10W
R 11	1	608-09-75001	624	RES, 75.0K 1% 1/10W
R 12	1	616-02-22009		RES,220 OHM 5% 1/4W

Table 6-21 (Cont d.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 14	1	608-09-14302	624	RES, 143.0K 1% 1/10W
R 15	1	608-01-49902	624	RES, 499K 1% 1/10W 100 PP
R 16	1	608-09-12701	624	RES, 12.7K 1% 1/10W
R 17	1	608-09-17401	624	RES, 17.4K 1% 1/10W
R 18	1	608-09-17401	624	RES, 17.4K 1% 1/10W
R 19	1	608-09-14300	624	RES, 1.43K 1% 1/10W
R 20	1	608-09-27401	624	RES, 27.4K 1% 1/10W
R 21	1	608-09-24901	624	RES, 24.9K 1% 1/10W
R 22	1	608-09-49900	624	RES. 4.99K 1% 1/10W
R 23	1	608-09-35701	624	RES, 35.7K 1% 1/10W
R 24	1	608-09-90900	624	RES. 9.09K 1% 1/10W
R 25	1	608-09-32401	624	RES, 32.4K 1% 1/10W
R 26	1	608-09-32401	624	RES, 32.4K 1% 1/10W
R 27	1	657-05-19601		RES, 19.6K .1% .12W
R 28	1	657-05-40009		RES, 400 OHM .1% .12W
R 29	1	657-05-40009		RES, 400 OHM .1% .12W
R 30	1	657-05-19601		RES, 19.6K .1% .12W
R 31	1	608-09-10002	624	RES, 100.0K 1% 1/10W
R 32	1	608-09-24902	624	RES, 249.0K 1% 1/10W
R 33 THRU R 35	3	616-02-20000		RES,2K 5% 1/4W
R 36	1	616-02-10005		RES, 100MEG 5% 1/4W
TP 1	1	143-98-00037		JACK,TEST BLACK .46 X.23
TP 2	1	143-98-00037		JACK,TEST BLACK .46 X.23
REF 1	1	905-01-00639	18881	SCHEMATIC,PWA
REF 2	1	905-04-00001	9500	SPEC,COMPONENT SPACING

Table 6-22

PARTS LIST 1373 REV DATE 03/14/74 REV LTR J

LIST TITLE PWA,REGULATOR CHGE CONT NO. CODE IDENT SHT 1 OF 3

PART NO. 205-89-01060 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	204-99-00695	1372	PWB,REGULATOR
2	4	298-98-00008		HTSK,FOR TO-5 PKG
3	3	189-99-00005	800-3	PAD,XSTR 8 PIN*USE CPTL*
4	1	298-99-00031	20648-1	HTSK,REGULATOR
5	2	189-98-00004		PAD,XSTR 4 PIN*USE CPTL*
6	2	189-99-00007	800-4	PAD,XSTR 10 PIN .075 HIGH
7	2	189-99-00001	800-1	PAD,XSTR TO-5,9 OR 11,4 P
8	AR	229-02-00075		SCREW,4-40X3/8 PAN HD
9	AR	287-02-00016		NUT,HEX,4-40 SST
10	AR	273-02-00025		WASHER,#4,INT TOOTH
11	AR	229-02-00073		SCREW,4-40X1/4 PAN HD
12	5	140-98-00007		INS,MICA TO-66 TRANSISTOR
13	AR	060-21-00002		CMPD,HEAT CONDUCTIVE GEL
C 1	1	304-08-04709	600	CAP. 47PF .5PF 500V
C 2	1	337-14-68003	601	CAP. 6.8MF 10% 35V
C 3	1	301-13-10002		CAP., .1MF 20% 50V LS.200
C 4	1	337-14-68003	601	CAP. 6.8MF 10% 35V
C 5	1	304-08-04709	600	CAP. 47PF .5PF 500V
C 6	1	337-14-68003	601	CAP. 6.8MF 10% 35V
C 7	1	337-14-68003	601	CAP. 6.8MF 10% 35V
C 8	1	339-12-15005	601	CAP., 150MF 10% 15V
C 9	1	301-13-10002		CAP., .1MF 20% 50V LS.200
C 10	1	304-08-04709	600	CAP. 47PF .5PF 500V
C 11 THRU	3	301-13-10002		CAP., .1MF 20% 50V LS.200
C 13				
C 14	1	301-03-10001		CAP., .01MF 20% 50V LS.10
C 15	1	301-03-10001		CAP., .01MF 20% 50V LS.10
C 16	1	301-06-00002		CAP,47PF 10% 100V
C 17	1	301-06-00002		CAP,47PF 10% 100V
CR 1	1	088-99-00099	642-00	DIODE,1N746A ZENER 3.3V
CR 2	1	088-10-47391		DIODE,9.1V 1W,SIM STD .4W
CR 3	1	088-10-09662		DIODE,VOLTAGE REG 16V 5%
CR 4	1	088-10-09642		DIODE,VOLTAGE REG.13V 5%
P 1	1	063-98-00162		CONN,RECP,52 POSN .150 SP
Q 1	1	263-97-00090		XSTR,NPN 60V,4A SW-AMPL
Q 2	1	263-97-00090		XSTR,NPN 60V,4A SW-AMPL
Q 3 THRU	3	263-10-37400		XSTR,PNP 60V,4A SW-DRIVER
Q 5				

Table 6-22 (Cont'd.).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
Q 6	1	263-10-29050		XSTR,PNP SW CR CORE DRIVE
Q 7	1	263-10-29050		XSTR,PNP SW CR CORE DRIVE
Q 8	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
Q 9	1	263-97-00093		XSTR,PNP,SWITCH/AMPL,50V
R 1	1	201-98-00014		POT., 500 OHM 10% 1W
R 2	1	622-02-00279		RES,2.7 OHM 5% 1/2W
R 3	1	608-01-03489	624	RES, 34.8 OHMS 1% 1/10W 1
R 4	1	616-02-06809		RES,68 OHM 5% 1/4W
R 5	1	201-98-00014		POT., 500 OHM 10% 1W
R 6	1	608-09-20000	624	RES. 2.0K 1% 1/10W
R 7	1	608-09-22601	624	RES, 22.6K 1% 1/10W
R 8	1	616-02-01009		RES,10 OHM 5% 1/4W
R 9	1	623-02-82009		RES. 820 OHM 5% 1W
R 10	1	608-09-16201	624	RES, 16.2K 1% 1/10W
R 11	1	608-09-20000	624	RES. 2.0K 1% 1/10W
R 12	1	616-02-06809		RES,68 OHM 5% 1/4W
R 13	1	622-02-00279		RES,2.7 OHM 5% 1/2W
R 14	1	623-02-68009		RES. 680 OHM 5% 1W
R 15	1	608-01-00000	624	RES,*TVAR* 1% 1/10W
R 16	1	616-02-10001		RES,10K 5% 1/4W
R 17	1	616-02-51000		RES,5.1K 5% 1/4W
R 18	1	608-09-28000	624	RES. 2.80K 1% 1/10W
R 19	1	608-09-51100	624	RES, 5.11K 1% 1/10W
R 20	1	608-01-01009	624	RES, 10.0 OHMS 1% 1/10W 1
R 21	1	622-02-10009		RES. 100 OHM 5% 1/2W
R 22	1	616-02-06809		RES,68 OHM 5% 1/4W
R 23	1	608-01-03489	624	RES, 34.8 OHMS 1% 1/10W 1
R 24	1	616-02-01009		RES,10 OHM 5% 1/4W
R 25	1	608-09-20001	624	RES. 20K 1% 1/10W
R 26	1	622-02-00279		RES,2.7 OHM 5% 1/2W
R 27	1	608-09-10500	624	RES, 1.05K 1% 1/10W
R 28	1	608-09-15001	624	RES, 15.0K 1% 1/10W
R 29	1	608-09-10500	624	RES, 1.05K 1% 1/10W
R 30	1	622-02-00279		RES,2.7 OHM 5% 1/2W
R 31	1	608-09-23700	624	RES., 2.37K 1% 1/10W
R 32	1	608-09-22100	624	RES., 2.21K 1% 1/10W
R 33	1	616-02-03309		RES,33 OHM 5% 1/4W
R 34	1	608-09-23700	624	RES., 2.37K 1% 1/10W
R 35	1	608-09-12100	624	RES. 1.21K OHM 1% 1/10W
R 36	1	616-02-03309		RES,33 OHM 5% 1/4W
R 37	1	201-98-00014		POT., 500 OHM 10% 1W
R 38	1	201-98-00089		POT., 2K 10% 1W
R 39	1	608-09-64900	624	RES, 6.49K 1% 1/10W
R 40	1	608-09-90900	624	RES. 9.09K 1% 1/10W

Table 6-22 (Cont'd,).

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
R 41	1	201-98-00089		POT., 2K 10% 1W
TP 1	1	143-98-00010		JACK, TEST, BLACK
TP 2	1	143-98-00009		JACK, TEST, RED
TP 3	1	143-98-00012		JACK, TEST, ORANGE
TP 4	1	143-98-00013		JACK, TEST, YELLOW
TP 5	1	143-98-00011		JACK, TEST, DARK GREEN
TP 6	1	143-98-00005		JACK,TEST,BLACK
U 1 THRU U 3	3	046-34-00011		INTCKT,VOLT REG POSITIVE
U 4	1	046-34-00008		INTCKT,NEG VOLT REGULATOR
U 5	1	046-34-00008		INTCKT,NEG VOLT REGULATOR
REF 1	1	905-04-00001	9500	SPEC,COMPONENT SPACING
REF 2	1	905-01-00748	1371	SCHEMATIC,PWB,REGULATOR

Table 6-23

PARTS LIST 13722
LIST TITLE SWITCH, ASSY, THUMBWHEEL
PART NO. 250-89-00014

REV DATE 03/14/74
CHGE CONT NO. CODE IDENT
ECO RECORD 1 06141

REV LETTER
SHT 1 of 1
CKD BY Braun

ITEM NO.	QTY REQ'D	EMR NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	250-98-00098		SW, THUMBWHL, BCD & CMPLM
2	8	088-97-02760		DIO, GE, SW, 100V, TRR 300 NS

FIRST USAGE MODEL 2746

Table 6-24

PARTS LIST 13722-1 REV DATE 03/14/74 REV LTR

LIST TITLE SWITCH,ASSY,THUMBWHEEL CHGE CONT NO. CODE IDENT SHT 1 OF

PART NO. 250-89-00024 ECO RECORD 1 06141 CKD BY

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	250-98-00098		Sw,THUMBWHL,BCD&CMPLM
2	4	088-97-02760		DIO,GE,SW,10CV,TRR 300NS

FIRST USAGE MODEL 515

PARTS LIST 13722-2 REV DATE 03/14/74 REV LTR E

LIST TITLE SWITCH,ASSY,THUMBWHEEL CHGE CONT NO. CODE IDENT SHT 1 OF 1

PART NO. 250-89-00027 ECO RECORD 1 06141 CKD BY Burr.

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	250-98-00098		SW,THUMBWHL,BCD&CMPLM
2	8	088-97-02760		DIO,GE,SW,100V,TRR 300NS
3	2	194-98-00007		PIN,STOP

FIRST USAGE MODEL 515

Table 6-26

PARTS LIST 13722-3 REV DATE 03/14/74 REV LTR B

LIST TITLE SWITCH,ASSY,THUMBWHEEL CHGE CONT NO. CODE IDENT 06141 SHT 1 OF 1

PART NO. 250-89-00028 ECO RECORD 1 CKD BY Bam

ITEM NO.	QTY REQD	E M R NUMBER	DRAWING OR SPEC NO.	DESCRIPTION
1	1	250-98-00098		SW,THUMBWHL,BCD&CMPLM
2	4	088-97-02760		DIO,GE,SW,100V,TRR 300NS
3	2	194-98-00007		PIN,STOP

FIRST USAGE MODEL 515

Table 6-27. Model 515-03 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
1	INTEGRATED CIRCUIT	046-97-00022	2	1	
2	INTEGRATED CIRCUIT	046-97-00035	5	1	
3	INTEGRATED CIRCUIT	046-97-00031	1	1	
4	INTEGRATED CIRCUIT	046-97-00029	2	1	
5	INTEGRATED CIRCUIT	046-97-00033	16	2	
6	INTEGRATED CIRCUIT	046-97-00034	56	6	
7	INTEGRATED CIRCUIT	046-97-00039	2	1	
8	INTEGRATED CIRCUIT	046-97-00102	15	1	
9	INTEGRATED CIRCUIT	046-97-00105	6	1	
10	INTEGRATED CIRCUIT, 4-Bit Binary	046-97-00107	1	1	
11	INTEGRATED CIRCUIT, 3 Transistor and 1 Diff.	046-15-00003	8	1	
12	INTEGRATED CIRCUIT, Op. Amp., 18V, V Out 2	046-16-00014	1	1	
13	INTEGRATED CIRCUIT, MA709C	046-18-00004	1	1	
14	INTEGRATED CIRCUIT, Diff. Comp. Gain 125	046-16-00014	1	1	
15	INTEGRATED CIRCUIT, High Volt. Hex Inv.	046-18-00015	16	2	
16	INTEGRATED CIRCUIT	046-34-00002	7	1	
17	INTEGRATED CIRCUIT, Voltage Comparator	046-34-00005	1	1	
18	INTEGRATED CIRCUIT, Voltage Comparator	046-34-00006	8	1	
19	INTEGRATED CIRCUIT, Voltage Follower	046-34-00007	8	1	
20	INTEGRATED CIRCUIT, Neg. Voltage Regulator	046-34-00008	2	1	
21	INTEGRATED CIRCUIT, Volt. Reg. Pos.	046-34-00011	3	1	
22	INTEGRATED CIRCUIT, Voltage Follower	046-34-00012	1	1	
23	INTEGRATED CIRCUIT, Op. Amp.	046-44-00002	1	1	
24	INTEGRATED CIRCUIT, Quad, 2-Input Pos.	046-97-00044	6	1	

Table 6-27 (Cont'd.). Model 515-03 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
25	INTEGRATED CIRCUIT, Hex Inverters	046-97-00047	4	1	
26	INTEGRATED CIRCUIT, Triple 3-Input Pos.	046-97-00050	1	1	
27	INTEGRATED CIRCUIT, Exp. 4 Wide, 2 In.	046-97-00058	1	1	
28	INTEGRATED CIRCUIT, Dual 4 In. Expander	046-97-00060	1	1	
29	INTEGRATED CIRCUIT, Dual Edge Trigger	046-97-00064	3	1	
30	INTEGRATED CIRCUIT, 4-Bit Binary Adder	046-97-00067	6	1	
31	INTEGRATED CIRCUIT, Decade Counters	046-97-00069	4	1	
32	INTEGRATED CIRCUIT, Sync 4-Bit Up/Down	046-97-00076	2	1	
33	LIGHT, Assembly, Decimal	155-89-00001	3	1	
34	LIGHT, Display, Red	155-98-00016	6	2	
35	FUSE, Slo-Blo, 1 Amp.	120-98-00020	1	5	
36	LAMP, T-1-3/4, 28V, 0.04A	151-02-00001	1	1	
37	METER, Edgewise, -100, -5, +1	170-99-00023	1	1	
38	METER, Edgewise, Green Ctr.	170-99-00026	1	1	
39	METER, Edgewise, Zero Ctr.	170-99-00027	1	1	
40	DIODE, Switch, 75V, TRR 4NS	088-10-09140	20	2	
41	DIODE, Ref. 11.7V/7.5 mA, 0.005%/°C	088-10-09420	1	1	
42	DIODE, Ref. 11.7V/7.5 mA, 0.002%/°C	088-10-09430	1	1	
43	DIODE, Voltage Reg. 13V ±5%	088-10-09642	1	1	
44	DIODE, Voltage Reg. 16V ±5%	088-10-09662	1	1	
45	DIODE	088-10-41480	14	2	
46	DIODE, Current Limiting	088-16-00089	1	1	
47	DIODE, Current Limiting	088-16-00099	1	1	
48	DIODE, 13.0V	088-16-47430	1	1	
49	DIODE, 1N746A, Zener, 3.3V	088-99-00099	1	1	
50	DIODE, 1N751A, Zener, 5.1V	088-99-00129	4	1	

Table 6-27 (Cont'd.). Model 515-03 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
51	DIODE, Ger. Switch, 100V, TRR, 1N276	088-99-00179	84	7	
52	DIODE, 1N752A, Zener, 5.6V	088-99-00199	1	1	
53	DIODE, 1N756A, Zener, 8.2V	088-99-00209	1	1	
54	DIODE, 1N758A, Zener, 10.0V	088-99-00259	12	2	
55	DIODE, 1N749A, Zener, 4.3V	088-99-00339	1	1	
56	DIODE, 1N755A, Zener, 7.5V	088-99-00299	1	1	
57	POTENTIOMETER, 500Ω ±10%, 1W	201-98-00014	9	2	
58	POTENTIOMETER, 1K ±10%, 1W	201-98-00015	3	1	
59	POTENTIOMETER, 200Ω ±10%, 1W	201-98-00029	2	1	
60	POTENTIOMETER, 5K ±10%, 1W	201-98-00033	1	1	
61	POTENTIOMETER, 20K ±10%, 1W	201-98-00040	2	2	
62	POTENTIOMETER, 1K ±10%, .75W, PC Mtg.	201-98-00138	1	1	
63	POTENTIOMETER, 200Ω Cermet PC	201-98-00160	1	1	
64	POTENTIOMETER, 1K 100 ppm Cermet, 20	201-98-00166	1	1	
65	POTENTIOMETER, 5K ±10% Cermet, 20T	201-98-00199	1	1	
66	RECTIFIER	214-98-00017	3	1	
67	SWITCH, Assembly, Thumbwheel	250-89-00024	2	1	
68	SWITCH, Thumbwheel, BCD, 10 Pos.	250-98-00015	3	1	
69	SWITCH, Toggle, SPDT	250-98-00025	2	1	
70	SWITCH, Toggle, DPDT	250-98-00088	3	1	
71	SWITCH, Thumbwheel, BCD, 10 Pos.	250-98-00098	10	2	
72	SWITCH, Rotary, 2 Pole/4 Pos.	250-98-00143	2	1	
73	SWITCH, Thumbwheel, Dbl. Width	250-98-00144	1	1	
74	SWITCH, Thumbwheel, 4 Pos./SP	250-98-00145	5	1	
75	SWITCH, PB, Lited, Altn., 2 Form Z	250-98-00044	1	1	
76	SWITCH, Rot., 2-Pole, 4 Pos./Sec.	250-98-00157	1	1	
77	TRANSISTOR, NPN 350 MHz, Sw.On 35N	263-10-08340	7	1	
78	TRANSISTOR	263-10-22700	1	1	

Table 6-27 (Cont'd.). Model 515-03 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
79	TRANSISTOR, NPN LL Chopper, HFE	263-10-24320	10	1	
80	TRANSISTOR, NPN LL Chopper, 45V	263-10-24321	16	1	
81	TRANSISTOR	263-10-25010	3	1	
82	TRANSISTOR, PNP LL Chopper, HFE	263-10-29451	19	2	
83	TRANSISTOR	263-10-30550	1	1	
84	TRANSISTOR, PNP, Switch/Amp., 50V	263-10-32510	56	5	
85	TRANSISTOR	263-10-37340	1	1	
86	TRANSISTOR	263-10-37400	3	1	
87	TRANSISTOR	263-10-39470	66	6	
88	TRANSISTOR	263-10-39560	4	1	
89	TRANSISTOR, SI FET, N Chan., Switch	263-10-43920	5	1	
90	TRANSISTOR, PNP Power, Amp./Switch	263-10-43980	1	1	
91	TRANSISTOR, SI PNP, Low Power	263-10-49380	2	1	
92	TRANSISTOR, Dual PNP, LL Diff.Amp.	263-16-00219	1	1	
93	TRANSISTOR, P Chan. Deplet Mode	263-16-00229	22	2	
94	TRANSISTOR, MOSFET P Chan. Dgtl.	263-45-00019	1	1	
95	TRANSISTOR, PNP Switch/Amp., 30V	263-97-49170	2	1	
96	TRANSISTOR, FET, N Channel	263-99-00419	1	1	
97	TRANSISTOR, PNP, Sw. or Core Drive	263-10-29050	2	1	
98	TRANSISTOR, NPN, 60V, 4A, Sw.-Amp.	263-10-37660	2	1	
99	TRANSISTOR, FET P Chan. Chopper	263-38-00019	8	1	
100	CAPACITOR, 4700 pF ±20%, 50V, LS.100	301-02-47000	2	2	
101	CAPACITOR, .047 μF ±20%, 50V, LS.1	301-03-47001	4	1	
102	CAPACITOR, 0.1 μF ±20%, 50V, LS.200	301-13-10002	18	2	
103	CAPACITOR, 0.47 μF ±20%, 50V, LS.20	301-13-47002	2	1	
104	CAPACITOR, 1.0 μF ±20%, 50V, LS.20	301-13-10003	1	1	

Table 6-27 (Cont'd.). Model 515-03 Recommended Spares List

ITEM NO.	PART DESCRIPTION	EMR STOCK NO.	TQ	RS	PRICE
105	CAPACITOR, 56 pF ±20%, 100V, Aged	341-06-05609	1	1	
106	CAPACITOR, 1100 µF $^{-10\%}_{+70\%}$, 50V	354-65-11006	2	1	
107	CAPACITOR, 2200 µF $^{-10\%}_{+75\%}$, 25V	354-69-22006	1	1	
108	CAPACITOR, 120 pF ±10%, 200V	363-34-12009	20	2	
109	CAPACITOR, 470 pF ±10%, 200V	363-34-47009	20	2	
110	CAPACITOR, 7360 pF ±1%, 50V	384-05-73600	1	1	
111	CAPACITOR, .0820 µF ±1%, 50V	384-05-82001	1	1	
112	CAPACITOR, .8200 µF ±1%, 50V	707-01-82002	1	1	
113	CAPACITOR, 47 pF ±.5 pF, 500V	304-08-04709	5	1	
114	CAPACITOR, 100 pF ±1%, 500V	304-20-10009	8	1	
115	CAPACITOR, 1000 pF ±1%, 100V	304-62-10000	7	1	
116	CAPACITOR, 3.3 µF ±10%, 15V	336-12-33003	21	3	
117	CAPACITOR, 2.2 µF ±10%, 20V	336-13-22003	12	2	
118	CAPACITOR, 1.0 µF ±10%, 35V	336-14-10003	27	3	
119	CAPACITOR, 6.8 µF ±10%, 35V	337-14-68003	4	1	
120	RESISTOR, 1Ω ±3%, .5W, 50 ppm	601-14-00109	2	1	
121	RESISTOR, Var., 25K ±10%, 2W	638-01-25001	1	1	
122	RESISTOR, 400Ω ±.1%, .12W	639-05-40009	2	1	
123	RESISTOR, 19.6K ±.1%, .12W	639-05-19601	2	1	
124	RESISTOR, 5.0K ±.01%, .3W	648-01-50000	2	1	
125	RESISTOR, 0.5Ω ±1%, 10W, 50 ppm	650-35-00059	1	1	

Table 6-28. Customer Provisioning Questionnaire

1. Equipment to be spared
   Model No.(s): _____
   Serial No.(s): _____

2. Number of equipments to be spared in each location _____

3. Operating time and cycle: _____ hours/day, _____ days/week.

4. Operating Environment:

   A. Temperature: _____
   B. Humidity: _____
   C. Altitude: _____
   D. Shock and Vibration: _____

5. Non-operating Environment: _____

   A. Temperature: _____
   B. Humidity: _____
   C. Altitude: _____

6. Desired probability of being able to spare from complement _____ percent for _____ months.

7. Can usage permit troubleshooting to parts level when a failure occurs? _____

8. What spare assemblies do you have that are used in this Model Equipment? _____

9. Do you wish us to exclude the EMR warranty period? _____

MP MASTER
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